Advancement on the Susceptibility of Analog Front-Ends to EMI

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Advancement on the Susceptibility of Analog Front-Ends to EMI

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A Morgana Bianca,
nata dalle acque
inondate di sole.
Coraggiosa scimmia
e leone ruggente,
gattina affettuosa
e fedele cane.
A te,
che sei fatta d'universo,
dono tutto ciò che
realmente ho e sono:
le mie parole
e i miei pensieri.

Summary

This thesis deals with the EMC characterization of analog front-ends, in particular the operational amplifier and the 2.4 GHz RF receiver. The former is largely used in electronic systems for its low-cost and versatility; it can be found almost in any front-end for signal conditioning, for example to accommodate the output of a sensor to the input of an analog to digital converter. The latter grows in importance for the Internet of Things applications being the 2.4 GHz Industrial, Scientific and Medical radio band licence free and widely used for wireless networking.

An initial objective of this study was to analyze the response of operational amplifiers to continuous wave interference referring in particular to the Direct RF Power Injection method. The upset induced by disturbance has been discussed by theoretical analysis, simulations and measurements. It has been found that small-signal models have limited validity in predicting the susceptibility of amplifiers.

The natural progression of this work was to analyze the response of amplifiers subjected to multi-tone disturbance. The upset of such interference has been found to be not only the generation of a DC offset but also the appearance of a low-frequency beat component in the case of intermodulation distortion.

This is an important issue for future research. On one hand, actual disturbance, intentional or unintentional RF emissions, are poorly described by the CW approach. It is sufficient to think about the wireless data transmissions. The RF emission for equipment based on the time division multiple access is mostly a high-frequency burst with a slow repetition rate. On the other hand, the interference injection test set-up can be modified by using an arbitrary waveform generator to measure and evaluate the response of both analog and digital circuits when subjected to actual interference.

Another important finding in this study was that 2.4 GHz transceivers were susceptible to low-frequency disturbance. Several interfering waveforms, not only the continuous wave, were injected directly in the receiver front-end once the wireless communication has been set. The measurement set-up was similar to the DPI method and results showed relevant errors for the square wave injection, even the interruption of the communication. The errors induced by the low-frequency interference were related to the time in which the input transistors of the LNA were

switched-off. If the LNA does not provide an useful signal for a time that is equal or greater than the symbol period, then the stages that follows in the receiver chain can't successfully decode the information.

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List of Symbols

f	Frequency of a periodic waveform
ω	Angular frequency
λ	Wavelength of a periodic waveform
c	The Speed of light
E	Electric field
Q	Total electric charge
q	Electric charge
ϵ_0	Permittivity of free space
C	Capacitance
V	Voltage difference
H	Magnetic field
I	Electric current
μ_0	Permeability of free space
φ	Magnetic flux density
L	Inductance
K	Inductive coupling coefficient
R	Resistance
Z	Impedance
Y	Admittance

A_d	Open loop gain of an Operational Amplifier
V_+	Voltage difference between OpAmp non-inverting input and ground
V_-	Voltage difference between OpAmp inverting input and ground
V_d	Differential voltage component of input voltage, $V_+ - V_-$
V_{cm}	Common mode component of input voltage, $(V_+ + V_-)/2$
GBW	Gain bandwidth product
SR	Slew rate
I_D	Drain current of CMOS transistor
V_{GS}	Gate to source voltage difference
V_{DS}	Drain to source voltage difference
V_{SB}	Source to body voltage difference
V_{TH}	Threshold voltage
V_{OD}	CMOS transistor overdrive voltage
μ_n	Electron mobility
C_{OX}	Gate oxide capacitance (per unit area) of a CMOS transistor
W/L	CMOS transistor aspect ratio. W and L are the gate width and length
g_m	Transconductance of CMOS transistor
r_0	CMOS transistor output resistance
g_{mb}	Backgate transconductance of CMOS transistor
I_C	Collector current of bipolar transistor
I_S	Reverse saturation current
V_{BE}	Base to emitter voltage difference
V_T	Thermal voltage
K_d	Transfer function relating V_+ and V_d in feedback OpAmp
K_{cm}	Transfer function relating V_+ and V_{cm} in feedback OpAmp
ΔV_{off}	Input referred offset voltage of an operational amplifier

V_p, I_p	Peak amplitude of an interfering waveform
a_n, ω_n	amplitude and angular frequency of an arbitrary tone
$\Delta f, \Delta\omega$	frequency and angular frequency spacing
$\|x\|, \angle(x)$	Magnitude and phase of x
P_{inj}	Injected power
S_{11}	Scattering parameter representing the voltage reflection coefficient at the port 1
Sen	RF receiver sensitivity
(S/N)	Signal to Noise ratio
k	Boltzmann constant
T	Temperature
B	Bandwidth of the RF receiver
NF	Noise Figure
G_n	Gain of an arbitrary block in the receiving chain
PER	Packet Error Rate
P_{ok}	Number of packets correctly received
$RSSI$	Received Signal Strength Indication

Introduction

Recent years witnessed the diffusion of electronic systems in every aspect of our life. The ability of electronics to switch and efficiently control electrical quantities has made possible both the processing of information and its exchange through telecommunication. Furthermore, electrical signals can be converted to other physical quantities by means of actuators, and vice versa, sensors can be used to acquire and translate information into electrical signals.

For example, light can be conveyed by lens to a photo-sensor matrix which converts photons into electrical charges or currents. Such analog signals are usually amplified and then translated, processed and finally memorized into the digital domain. The information can also be used to properly drive a matrix of light emitting diodes; in this way a photographer can directly check on the back display of its digital camera the captured image.

Modulated electromagnetic waves can be picked up by antennas, decoded and converted by an electro-acoustic transducer, i.e. the loudspeaker, into sound. This is an illustration of how it is possible to listen to the music transmitted by a broadcasting station. Applications of electronic systems is limited only by the human imagination, in fact they are widely employed for purposes such as computation, communication, process automation and so on. The widespread use of electronics has resulted in several appliances to operate in close proximity, possibly affecting each other in an negative way. Every active device and moving charges within conductors generate electromagnetic (EM) fields. These waves can couple with wires, conducting plates or traces, and be conveyed in the form of electrical quantities to other circuits. Moreover, electronic devices are affected by intrinsic noise sources, e.g. thermal or flicker noise, and by natural EM disturbance, e.g. the one caused by sunspots or lightening.

Even in the presence of such an adverse environment, electronic systems have to work properly and not be a source of electromagnetic pollution. If these requirements are met, the equipment is said to be compatible in its EM environment. For this reason, the field of study that concerns emissions, propagation and reception of the EM energy is called electromagnetic compatibility (EMC).

EMC grown in importance through years and despite decades of investigations

it is an ongoing research field: it is critical for the reliability of devices. The EMC issue should be addressed at early design stage; as long as the development of the electronic system progresses to production, techniques to mitigate EMC problems decrease steadily [1]. If a circuit is adversely affected by the EM field or noise, it is said to be susceptible to electromagnetic interference (EMI).

Chapter 1 addresses the problem of interference which is defined by three elements: the source of EM emissions, a coupling path and the receptor circuit.

Standard measurement methods have been developed by international standardization committees rather than electronic companies associations with the aim of ensuring the robustness and the reliability of electronic systems. These regulations deal with two main factors: the emission of electromagnetic energy and the immunity to that energy. The former is controlled by setting limits to the maximum allowable emitted energy while the latter specifies the EM environment in which the equipment works as intended, i.e. with no degradation in its functionality. EMC test and measurement setups are defined, e.g., by the International Electrotechnical Commission [2] in standards such as the IEC-61967 (that deals with EM emission), the IEC-62132, IEC-62215 and IEC-61000, that concern the susceptibility of IC to Radio Frequency Interference (RFI), to impulses and to Electro Static Discharge (ESD) respectively. Other standards have been published by the International Special Committee on Radio Interference (CISPR) or by the International Organization for Standardization [3].

Standards became also directives of conformity; electronic circuits that are not compliant with EMC directives cannot be legally sold and thus they have to be redesigned. All electronic appliances, from system level down to the Integrated Circuit (IC) level, must comply with EMC constrains. Their characterization has become essential but it is still challenging, especially for modern ICs which encapsulates several chips within the same package. On one hand there is the need of the modeling of the disturbance coupling rather than the RFI injection path; on the other hand the computer simulations, usually in time domain, require huge computational time due to the increased complexity.

Based on the fact that interface cables are responsible to conduct interference within electronic equipment, the interface circuits, i.e. analog front-ends, should receive the first attention. Chapter 2 deals with the analysis of a susceptible building block widely used in analog circuits, i.e. the Operational Amplifier. One of the most known testing procedure, the Direct RF Power Injection, is taken as reference and a method to model the injection path and the device under test is also presented. Such work has been presented at the 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo 2015, Edinburgh, UK) [4].

In the following Chapter 3, the EMI Rejection Ratio, a parameter introduced by Texas Instrument with the attempt of qualifying the susceptibility of OpAmps, is discussed. Such parameter has started to appear also in datasheets as a figure of

merit in terms of EMC. It has been shown by means of analysis and measurements on commercially available OpAmps that its validity is limited to low-amplitude interfering signal only [5].

Despite the usefulness of EMC tests for design verification and validation, some criticisms arose in the literature [6]-[8]. It has been pointed out that EMC testing does not cope well with real-life EM environment (e.g. simultaneous EM threats such as a radiated field and an electrostatic discharge) and the standards shall be reviewed by increasing the immunity test level or by adopting non-standardized immunity testing, especially for safety-related appliances. To this purpose the investigation of the effects induced by multi-tone interference in feedback Operational Amplifiers has been presented at the 13th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME 2017, Giardini Naxos, Italy). Under the assumption of weak non-linearity, an analytical model is derived to predict the output offset induced by the superposition of an arbitrary number of sinusoidal disturbance and to evaluate the intermodulation distortion caused by two-tone interference [9]. The natural progression of such work was the testing of commercially available OpAmps subjected to multi-tone interference. An interesting comparison between the effects induced by the injection CW signals and two-tone interference, together with an affordable test setup to perform a wide-coverage susceptibility testing, has been presented at the 2018 Joint IEEE EMC & APEMC Symposium [10].

Also the susceptibility of 2.4 GHz ISM band receivers has been reviewed in the low-frequency range. Existing standard such as the ETSI EN 300 328 or the wireless specifications only deal with CW interference with frequency from 30 MHz to 12.75 MHz; especially the Bluetooth core specification, which is the more stringent one. Neither measuring standards nor investigations concerning the immunity of transceivers to lower-frequency interference are available yet. The work was based on the assumption that practical power switching circuits generate interference with frequency components below such minimum frequency. The disturbance coupled onto the receiving path can reach the inputs of the Low Noise Amplifier (LNA) leading to communication impairments. The reliability of Bluetooth Low Energy (BLE) receivers in presence of low-frequency disturbance has been discussed in [11] (IEEE Transactions on Electromagnetic Compatibility) and a comparison between the two most known low-energy wireless technologies operating in the 2.4 GHz band, i.e. BLE and the Zigbee, has been presented at the 2018 Joint IEEE EMC & APEMC Symposium [12]. Measurement results pointed out vulnerability of receivers to injected interference; in particular square waves with amplitude of hundreds of millivolts and frequency ≤ 1 MHz practically interrupt the wireless communication. The investigation pointed out the need to focus more in the low-frequency range when RF transceivers are designed and tested.

Chapter 1

The problem of interference

Latest advancement in electronics comprised the increasing of speed, the reduction of the power consumption and the shrinking of the products size. More and faster circuits can be embedded into less space (e.g. systems on chip or system in package) providing more functionalities. Furthermore, the low power consumption increases the life of portable equipment batteries. As a consequence such apparatus has become more appealing to the market. These trends are not positive from the EMC point of view. On one hand, lowering the power implies lower functioning margins, on the other hand the crowding of circuit in small space increase the probability of interference.

As already mentioned, the interference problem needs at least three basic elements to be defined. This is shown in the block diagram of Fig.1.1 where, from left to right, there are the interference source which emits or conducts electromagnetic energy, the coupling path and finally the receptor which process the conveyed energy. For example, in mixed signal ICs, the switching of digital circuits generates disturbance that can reach susceptible analog circuits through the supply network or the common substrate. If the effect of such received EM energy is adverse to the functioning of the receptor circuits, then there is an interference problem. The interference is effective if

- it is emitted at a frequency that the receptor is susceptible of (e.g. the desensitization of a radio receiver in presence of a strong signal with frequency lying within the communication bandwidth)
- the received signal amplitude is high enough to affect the receptor. An example is the change of the operating region of transistors when subjected to RFI [13]
- the disturbance affect the receptor at the time in which it is designed to work. If an interference capable of switching off the receptor circuit is received when the circuit is already powered off, then there is no interference problem.

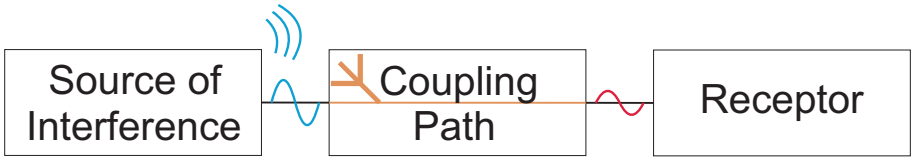


Figure 1.1: Block diagram representing the interference problem.

Three ways lead to the solution of the problem, the first is the suppression of the interference source or the change of its characteristic with the aim of making the disturbance less effective. Secondly the transmission of the EM energy by means of the coupling path can be minimized or mitigated (e.g. by properly shielding emitting cables). Last but not least, the receptor can be designed to be hardened against interference.

1.1 Sources of interference

The electromagnetic pollution is caused by natural phenomena, especially lightning, but mostly by man-made devices. Disturbance covers almost all the frequency spectrum and can be classified as narrow-band or broad-band. An example of the former is the emission from high-voltage power lines which emits prevalently around the power frequency (50 Hz in Europe). Also radio broadcaster and wireless communication devices transmit information modulated onto a carrier frequency, and thus the spectrum of their emissions is located around this frequency. Broader spectrum interference, instead, are emitted by switching-mode power supply, relays or motor drivers.

Other switching circuits widely used in ICs are those employed in digital logics, which is the core of any processing element. Information is managed by means of two levels, the high level representing the binary number 1 and the low level the number 0. Digits, and changes from one digit to the other, are therefore handled by the transmission of pulses as depicted in Fig.1.2. Three waveforms are plotted in the time domain: the square wave (in blue) and the triangular wave (in red) are the two extremes representing the fastest and the slowest transition times for a given frequency and amplitude. In the middle there is the trapezoidal wave, which is the best actual representation of digital pulses. The time domain characteristics of pulse trains, especially the rise and the fall time, determine the spectral contents (faster transitions implies EM emissions in a broader range of frequency).

In Fig.1.3(a) there are the frequency domain representations (Fourier transform) of the pulse trains depicted in Fig.1.2. Fig.1.3(b) represents the asymptotic envelope which bounds the spectral contents of the digital pulse trains. These envelopes show

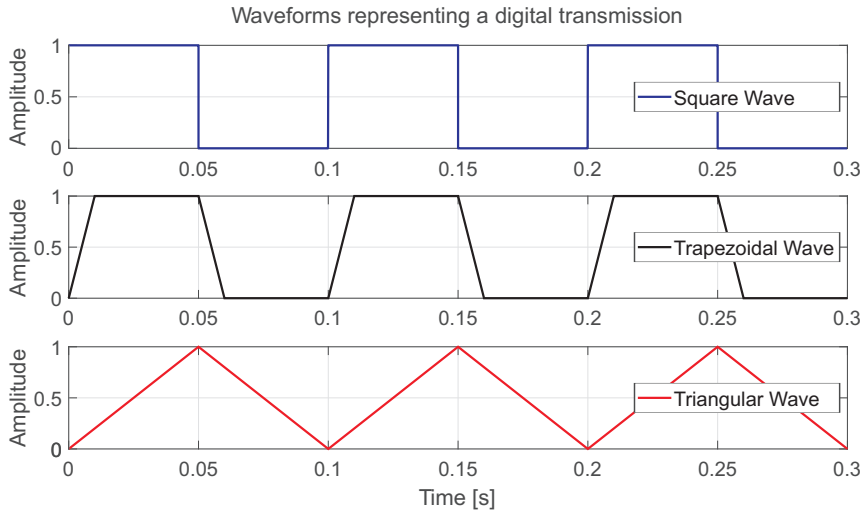
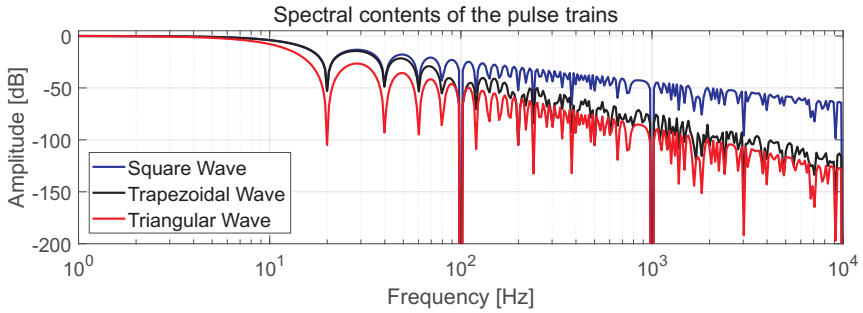
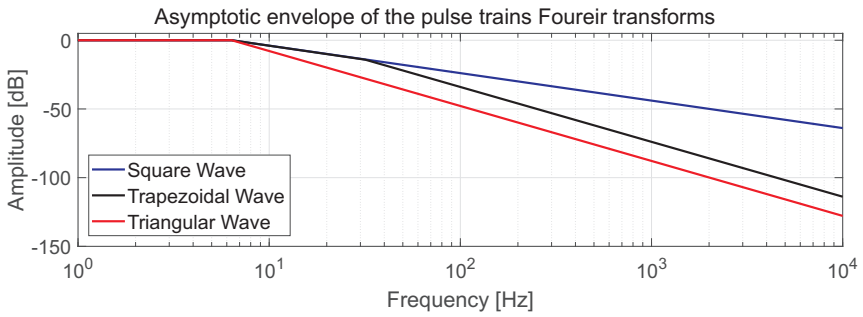


Figure 1.2: Representation of digital pulses in time domain.



(a)



(b)

Figure 1.3: Representation of digital pulses in frequency domain. Fourier transform (a) and asymptotic envelope (b).

the pole locations and the trends of the corresponding waveforms. The square wave present a single pole (at $1/(\pi\tau)$ where τ is the time period in which the signal is

high) and a roll-off of −20 dB. The triangular wave has two poles at the same frequency and a roll-off of −40 dB. The finite rise time τ_r of the trapezoidal wave, with respect to the square wave, introduces a second pole located at $1/(\pi\tau_r)$, thus a roll-off of −40 dB for higher frequency. The reduction of the rise and fall times, therefore, implies a reduction of the high-frequency spectral components, as well as of the high-frequency EM emissions.

However, it is not always possible to mitigate or suppress emissions of an interference source. It is the case of intended RF transmitters such as radars or wireless communication devices whose functioning is actually based on the transmission (and reception) of electromagnetic waves. The interference problem should then be addressed analyzing and minimizing the effect of the coupling path or making the receptor immune to that disturbance as briefly discussed in the next sections.

1.2 Coupling path

The coupling path describes how the electromagnetic environment is translated into disturbing signals (usually electrical quantities) at the receptor circuit or within it. Interference can be caused by conducted or radiated energy or by both. Conductive coupling can occur when the current of different circuits flows into the same impedance (e.g. ground or supply lines networks). Each circuit sees a voltage drop across it that is influenced by other circuits possibly interfering with its correct operations.

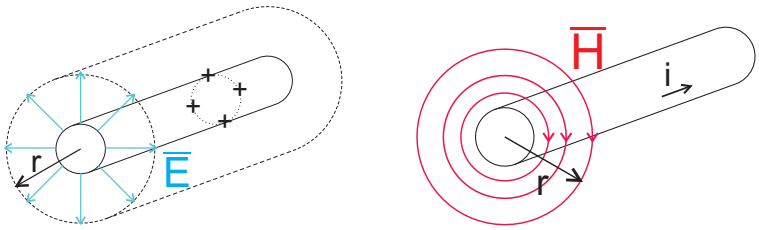
Interference can be conveyed to the victim also by means of wires and signal traces, and the radiation and the reception of EM waves is probably one of the most troublesome and time consuming issue. Exact solutions can be achieved only by the solution of Maxwell's equations, a quite complicated four dimensional problem (3 space variable plus time). However, if the largest physical dimension of the circuit is smaller than the wavelength of the disturbance signal involved, then the spatial variables can be eliminated leading to solutions that are function of the time only. With this approximation, the coupling path can be described by lumped elements and the network theory can be used for a less complex analysis. For example, dealing with the EMC of integrated circuits, the maximum interfering frequency to be applied is 1 GHz. The corresponding wavelength (λ = speed of light divided by frequency) is 30 cm and circuits with dimension smaller than 3 cm ($\lambda/10$) can be considered electrically small.

Nevertheless, PCB tracks and wires are usually the longest part of circuits; they operate as unwanted antennas which pick up radiated energy and conduct such interference to the attached circuit, i.e. the analog front-end. Moreover, the strength of the electromagnetic field decreases as the distance increases, therefore one solution to make the coupling path less effective could be to increase the spacing between

the EM source and the receptor. Oddly, wires and interconnects, especially for devices with large number of input/output ports, lie close to each other and their reciprocal influence (crosstalk) has to be addressed, in particular, in the PCB layout. In the following subsection the electromagnetic coupling between wires is solved analytically to gain an insight in the basic mechanism. The low-frequency lumped-element approximation presented hereinafter have been used in chapter 5 to derive a model describing the low-frequency coupling between an interfering wire and two PCB printed antennas.

1.2.1 Electromagnetic coupling

Two subproblem are the basis for the electromagnetic analysis of wires [14]: the first is related to the electric field around a wire with uniform charge distribution and the induced voltage, the second deals with the magnetic field and the magnetic flux through a surface.



(a) (b)

Figure 1.4: Representation of electric field (a) and magnetic field (b) around a wire.

The electric field E is calculated by the Gauss'law; it states that the electric flux exiting a closed surface S is proportional to the total enclosed charge Q. In integral forms it reads:

$$\oint_S E \cdot ds = \frac{Q}{\epsilon} \tag{1.1}$$

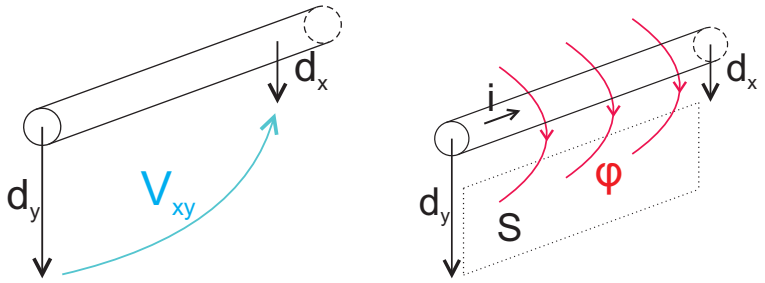
where ϵ is the permittivity of the surrounding medium. The electric field can be calculated analytically in the case of a wire suspended in free space ($\epsilon = \epsilon_0 \approx 8.854 \times 10^{-12} F/m$) and assuming that the positive per unit length charge is uniformly distributed in the wire periphery. The closed surface that has been chosen is a cylinder with radius r as shown in Fig.1.4(a). The resulting electric field is transverse to the wire and directed outward (blue arrows); its magnitude in V/m, according to [14], is derived to be:

$$E = \frac{q}{2\pi\epsilon_0 r}. \tag{1.2}$$

The electric field is null within the wire and constant over circles concentric with the wire cross section (equipotential lines). Therefore, the voltage of two points

having the same radial distance from the wire will be 0 V, indeed they lie on the same equipotential line. On the other hand, if their distances (with respect the wire axis c_0) differ, the voltage is evaluated by the difference of their electric potential. Suppose the point y more distant with respect the point x, i.e. $d_y > d_x$ as shown in Fig.1.5(a); the voltage V_{xy} become:

$$V_{xy} = -\int_{c_0}^{d_x} E \cdot dl + \int_{c_0}^{d_y} E \cdot dl = \int_{d_x}^{d_y} \frac{q}{2\pi\epsilon_0 r} dr = \frac{q}{2\pi\epsilon_0} ln\left(\frac{d_y}{d_x}\right) \tag{1.3}$$



(a) (b)

Figure 1.5: Representation of basic problems: voltage difference between two points near a charged wire (a) and magnetic flux density through a surface near a wire carrying current (b).

The magnetic field H is handled by the Maxwell-Ampere's law; it relates the magnetic fields integrated over a closed contour C with the current I flowing trough such loop. Omitting the displacement current (dependent on the time variation of the electric field enclosed by the same contour) it can be written as:

$$\oint_C H \cdot dl = I. \tag{1.4}$$

The current is assumed to be uniformly distributed within the wire and the chosen closed contour is a circle concentric with the wire cross section as shown in Fig.1.4(b). The magnetic field results to be tangent to the circle (the direction is governed by the right hand rule) and constant at the circumference (red lines). Moreover, the magnitude (in A/m) of the magnetic field decreases linearly with the increasing of the circle radius r:

$$H = \frac{I}{2\pi r}. \tag{1.5}$$

In the case of free space or non-ferromagnetic material, the magnetic flux density equals the magnetic field multiplied by the permeability $\mu_0 = 4\pi \times 10^-7 H/m$, i.e.

$B = \mu_0 H$. Its integration over the surface S, see Fig.1.5(b), serves to derive the total magnetic flux density φ penetrating such surface, that is:

$$\varphi = \int_S B \cdot ds = \int_{d_y}^{d_x} \frac{\mu_0 I}{2\pi r} dr = \frac{\mu_0 I}{2\pi} ln\left(\frac{d_y}{d_x}\right). \tag{1.6}$$

The solutions of the two basic problems can be used to derive not only the per-unit-length parasitic capacitance and inductance of wires (and combinations of parallel wires) but also the mutual parasitics that are the main contributors in the coupling between conductors.

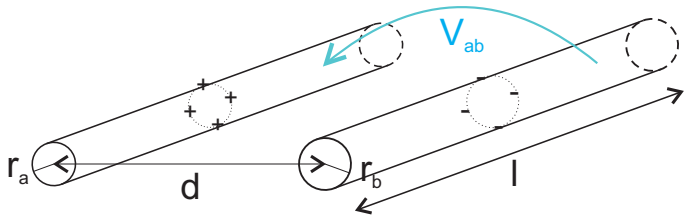


Figure 1.6: Geometry for the mutual capacitance evaluation.

For example, the mutual capacitance between two parallel cables can be evaluated referring to Fig.1.6. Wires have different radii (r_a and r_b) and they are separated by a distance $d \gg r_a, r_b$, so the proximity effect can be neglected. Their mutual capacitance is defined as the per-unit-length charge (uniformly distributed in the periphery) divided by their voltage difference. The voltage difference is derived from Eqn.(1.3) to be:

$$V_{ab} = \frac{q}{2\pi\epsilon_0} ln\left(\frac{d - r_b}{r_a}\right) + \frac{q}{2\pi\epsilon_0} ln\left(\frac{d - r_a}{r_b}\right) \approx \frac{q}{2\pi\epsilon_0} ln\left(\frac{d^2}{r_a r_b}\right) \tag{1.7}$$

and the mutual capacitance become:

$$C_m = \frac{2\pi\epsilon_0 l}{ln[d^2/(r_a r_b)]} \tag{1.8}$$

where l is the length of cables. A similar result applies also for the external inductance of the two wires, defined as the ratio of the flux entering the surface between cables and the current:

$$L_{ext} = \frac{\mu_0 l}{2\pi} ln\left(\frac{d^2}{r_a r_b}\right) \tag{1.9}$$

By adding a third cable it is possible to derive the mutual inductance between an interferer and a receptor wire sharing the same current returning wire. The geometry

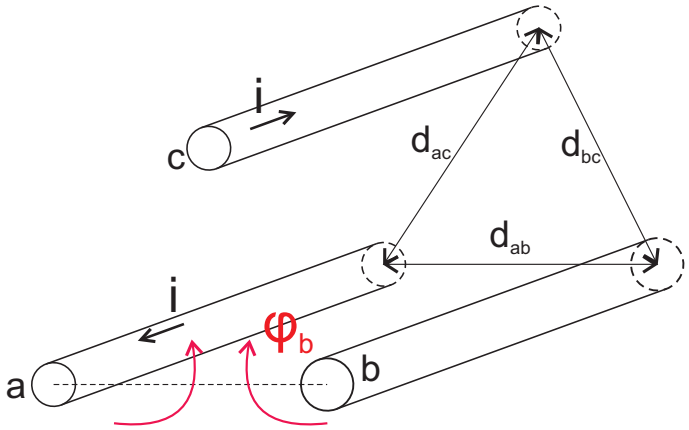


Figure 1.7: Geometry for the mutual inductance evaluation.

of the problem is depicted in Fig.1.7 Considering a as the returning current wire, the per-unit-length inductances are evaluated as follows:

$$l_c = \left.\frac{\varphi_c}{I_c}\right|_{I_b=0} \qquad l_m = \left.\frac{\varphi_b}{I_c}\right|_{I_b=0} \tag{1.10}$$

$$l_b = \left.\frac{\varphi_c}{I_b}\right|_{I_c=0} \qquad l_m = \left.\frac{\varphi_b}{I_b}\right|_{I_c=0} \tag{1.11}$$

$$\tag{1.12}$$

where l_c and l_b are the per-unit-length self-inductances of wire c and b respectively. The self-inductance of wires with length l (i.e. $L_c = l_c l$) are found applying the current on the referred wire and setting the other one to zero [14]:

$$L_c = \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ac}}{r_c}\right) + \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ac}}{r_a}\right) = \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ac}^2}{r_a r_c}\right) \tag{1.13}$$

$$L_b = \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ab}^2}{r_a r_b}\right) \tag{1.14}$$

Similarly, the mutual inductance is found by applying the current to one circuit, e.g $I_b = 0$ and evaluating the flux entering the surface between wire b and a (red arrows):

$$L_m = \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ac}}{d_{bc}}\right) + \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ab}}{r_a}\right) = \frac{\mu_0 l}{2\pi} ln\left(\frac{d_{ac} d_{ab}}{d_{bc} r_a}\right) \tag{1.15}$$

1.2.2 Low-frequency lumped-element approximation

The mutual capacitance and inductance can be used to derive the per-unit-length equivalent circuit, and thus to build up the distributed model representing the coupling between wires. For weakly coupled lines, the coupling is a linear combination

of the mutual inductance and the mutual capacitance. The capacitive coupling dominates in the case of a wire loaded with an high impedance while the contribution of the inductive coupling is predominant in the case of low impedance loads [14]. Furthermore, if the circuit is electrically short, the mutual capacitance and inductance characterize also the lumped element model as presented in the simplified equivalent circuits of Fig.1.8(a) and (b).

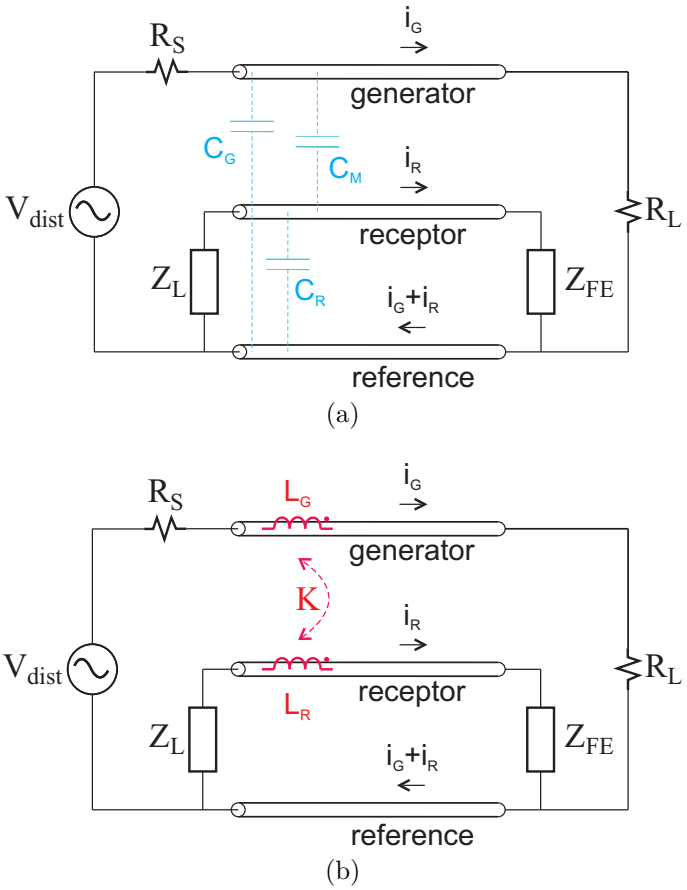


Figure 1.8: Low-frequency lumped-element equivalent circuit representing the electromagnetic coupling between wires. Capacitive coupling (a) and inductive coupling (b) simplifications.

The voltage generator V_{dist} is used to represent a disturbance source; the voltage and the current i_G on the generator line are primarily determined by the source and the load resistance (R_S and R_L). The receptor line, on the other hand, is loaded both sides by Z_L and Z_{FE} representing the load of the line and the input impedance of the analog front-end.

The electric field coupling, Fig.1.8(a), is represented by C_G and C_R that are the

self (or stray) capacitance of the generator line and of the receptor line and by C_M which is the mutual capacitance. The magnetic field coupling, Fig.1.8(b), can be described by two coupled inductors. L_G and L_R are the self inductances of generator and receptor lines respectively, while the mutual inductance here is hidden within the coupling coefficient K.

The solution of such equivalent circuits allow the derivation of the interference propagating from the source to the inputs of the front-end. Viceversa, if the susceptibility of the front-end is known, it can be used to derive which is the maximum acceptable level of interference at the source.

1.3 Receptor circuit

The last actor involved in the interference problem is the receptor circuit. Any electronic designer should bear in mind that all circuits are susceptible to interference, both digital and analog ones.

RF disturbance coupled onto binary data links can cause false commutations or timing errors. The first impairment is strictly related to the noise margin of the digital receiver: it specifies voltage thresholds for what is correctly received as '1' or '0'. A disturbing signal exceeding such margin may lead to false commutations. The latter is of particular interest for tightly time-constrained circuits; the jitter caused by the interference can upset the proper communication [15].

In the same way, interference corrupts the nominal functioning of analog comparators leading to false commutations, whenever the frequency is lower than the inverse of the comparator's delay, or affecting the threshold. This phenomenon has been ascribed to the DC offset shift induced by the rectification of higher frequency interference [16]. The same upset has been observed in bandgap references, low dropout voltage regulators, current sensor and in general in all those circuits employing operational amplifiers [17].

Chapter 2

EMC of Operational Amplifier

Amplification is one of the primary task that a signal processing chain has to perform. For example, the output of transducers is usually conveyed by weak electrical signals and it is better processed if its magnitude is made larger, i.e. by using a signal amplifier. The main function of such building block is to provide a suitable (and magnified) replica of its input signal to the stages that follow, e.g. the accommodation of a sensor's output to the input of an analog to digital converter. Any degradation in its output signal leads to the processing of a corrupted information, resulting in malfunctions or errors in the acquisition system. Thus the distortions of amplifiers are of particular concern.

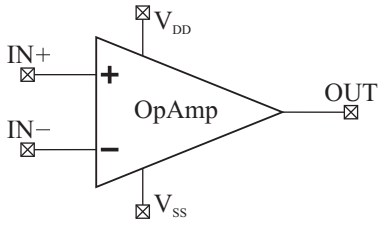


Figure 2.1: Symbol of the Operational Amplifier.

Over the years, the Operational Amplifier has become very popular and a widespread building block in analog design due to its versatility and ease of use. The most general and known symbol for the OpAmp is depicted in Fig.2.1; it has 5 terminals, usually two are used for the positive and negative DC power supplies (V_{DD} and V_{SS} respectively) and the other three for the signal amplification. In particular, the output voltage V_{OUT} is related to the difference of input voltages by

$$V_{OUT} = A_d \, (V_+ - V_-) \tag{2.1}$$

where the term A_d represents the open loop gain of the amplifier, ideally supposed infinite. Other characteristics of the ideal OpAmp are the infinite input impedance

(no current flowing into input terminals), zero output impedance (output voltage independent of the loading), infinite common mode rejection (amplification of the differential voltage only) and infinite bandwidth. Nowadays, high quality OpAmps are commercially-available even at low price. Characteristics such as open loop gain higher than 100 dB, input current lower than nH, input impedance in the GΩ range and gain bandwidth product of 1 MHz can be easily found.

OpAmps can be used in open-loop acting as comparators; the output voltage clips to the positive or negative supply voltage whether the voltage at the non inverting input is greater or lower than the voltage at the inverting terminal. Nonetheless, operational amplifier are usually connected in close loop by means of negative feedback trading the high gain for the improvement of performances such as the reduction of the non-linearity distortions, the increasing of the bandwidth and also enhancing input and output impedances. The negative-feedback together with the high open-loop gain are basically used to reduce the sensitivity to manufacturing or environment variations. Consider as an example the inverting amplifier shown in Fig.2.2.

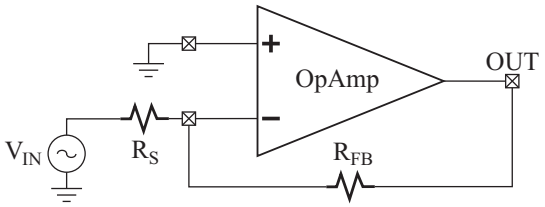


Figure 2.2: Schematic of the inverting amplifier.

This kind of amplifier is made by connecting a feedback resistor R_{FB} between the output terminal and the inverting input and feeding the amplifier at the same input by means of a voltage generator and a series resistor R_S. The infinite open loop gain and the negative feedback force the same voltages at the input terminals, i.e. $V_{IN+} = V_{IN-} = 0\,\mathrm{V}$; the inverting terminal is said to be a virtual ground. The current flowing through R_S and consequently through R_{FB} will be V_{IN}/R_S, meaning that the voltage at the output node will be the inverse of the ratio between the feedback resistor and the series one. Considering the OpAmp with finite gain, the voltage at the inverting terminal, derived from Eqn.(2.1), is $-V_{OUT}/A_d$, The current trough R_S become $(V_{IN} + V_O/A_d)/R_S$ and the gain of the amplifier is found to be

$$\frac{V_{OUT}}{V_{IN}} = \frac{-R_{FB}/R_S}{1 + (1 + R_{FB}/R_S)/A_d}. \tag{2.2}$$

Manufacturing process and temperature variations cause, e.g., the open loop gain of different OpAmps not to be the same, but as long as $A_d \gg (1 + R_{FB}/R_S)$ the voltage gain of the inverting amplifier become practically $-R_{FB}/R_S$, thus not

sensitive to those variations but only to the feedback network. This is the base of all circuits employing operational amplifiers and negative feedback and it has been made possible by actual OpAmps, which have characteristics close to the ideal ones.

This building block has been widely used in analog circuits since a wide variety of functionalities can be accomplished: OpAmps can be used for the design of integrators or differentiators, active filters, linear or non-linear amplifiers, precise rectifiers and so on. They can be found as stand-alone components or as functional blocks embedded within ICs.

Oddly, analog circuits, and in particular OpAmps, are proved to be very susceptible to interference coupled onto their input terminals. Moreover, the EMC issue have become a figure of merit for the selection of OpAmps; the need for low EM emission and susceptibility has resulted in the need of understanding and characterizing ICs in terms of EMI. Such characterization is usually a challenging and time consuming task. The small-signal analysis, indeed, has limited validity because, on one hand, non-linearities causes the main unwanted effects such as cross modulation, intermodulation, rectification, etc. [18]. On the other hand, interference reaching the IC inputs can be in the order of Volts in magnitude, thus possibly leading transistors out of their designed operating region. The time-domain transient analysis are the best simulations to predict the susceptibility of integrated circuits. The harmonic balance method can be an alternative for reducing the computational time [19]. Another way to simplify the analysis is the use of macromodels obtained via circuit simplifications; it has been proposed in early works of Graffi, Masetti et al. [20]. The advantage of the computational time reduction is also the possibility to make extensive simulations, thus covering wide case studies. A simple model of a CMOS OpAmp is shown in section 2.1 and it has been used for simulating and analyzing the upset induced by RF interference.

The main effect arising from the application of disturbance onto the input terminal of a feedback OpAmp is the generation of a DC offset shift in the output node. Such perturbation limits the reliability of electronic circuits employing operational amplifiers and its causes were investigated in past years [21]-[25]. A review of the two root causes is presented in section 2.2.

In addiction, the susceptibility profile of ICs shall be evaluated according to EMC directives such as the IEC-62132 which specifies the measurement of electromagnetic immunity of ICs in a frequency range comprised from 150 kHz to 1 GHz. The Part 4 [26] concerns the Direct RF Power Injection (DPI) method and this measurement technique is widely employed due to its ease of use. Moreover the DPI testing method can be simulated [27]-[28] and EMC specifications (usually at PCB level) can be translated to pin specifications; it allows the analysis and the design of robust devices. However, the analysis of the propagation of disturbance from the injection point to the susceptible subcircuit within modern ICs can be challenging. To this purpose, an effective method to model an IC which encloses two separate dies and

to analyze the interference propagation to the inputs of an OpAmp used for current sensing is presented in Section 2.3.

2.1 OpAmp model

To get further insight into the upset induced by RFI coupled onto the amplifier's input pins, a practical model of an OpAmp is designed, analyzed and widely simulated. The typical structure of an operational amplifier can be subdivided in three main stages, the first takes the input voltages and usually converts them into a differential current. The most used building block performing such operation is the differential pair and it is made up of two transistors connected together and biased by a constant current source. In the next stage, the differential current is converted in a single ended voltage by means of a high-gain transimpedance stage, e.g. by a folded cascode circuit. The last stage works as a buffer, transforming the usually high output impedance of the previous stage in the required low output impedance of the operational amplifier. Such output stage is not strictly necessary, for example, for only capacitive loaded amplifiers for which the output impedance can be high.

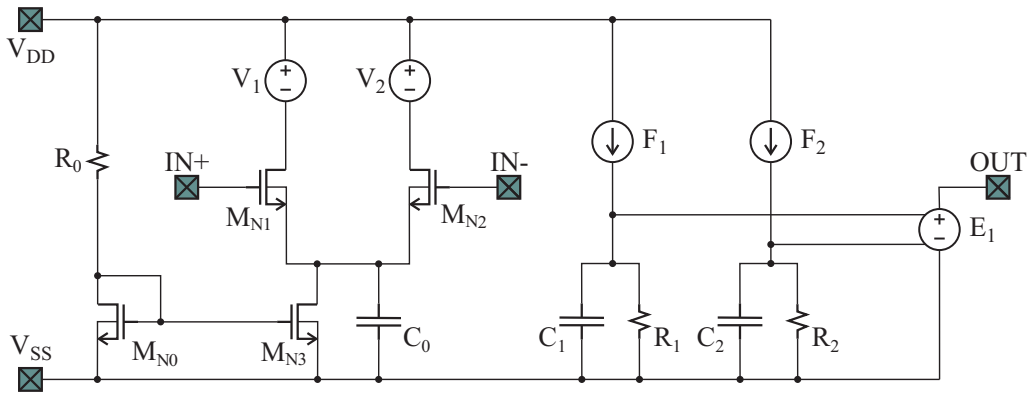


Figure 2.3: Schematic of the modeled Operational Amplifier.

The OpAmp simulated in this work is depicted in Fig.2.3. The same terminals of the circuit symbol of Fig.2.1 are evidenced: on the left there are the positive and negative power supplies V_{DD} and V_{SS}. The two terminals named $IN+$ and $IN-$ are the non-inverting input and for the inverting input respectively. These terminals are directly connected to the gates of two nMOS transistors of the differential pair. The process, 0.35 µm CMOS [29], has been chosen since it allows the integration of both the analog and the digital circuits within the same low-cost IC. In particular, the differential pair transistors ($MN1$ and $MN2$) are made up of two isolated nMOS allowing the connection of the body to the source (and not to the lowest voltage V_{SS}), thus avoiding the body effect. Input transistors are biased by the current mirror

composed by standard nMOS transistors $MN0$ and $MN3$; the use of the isolated counterpart is not strictly necessary, indeed their sources are connected to V_{SS}. An unbalance in the differential input voltage $V_d = V_{IN+} - V_{IN-}$ leads to a differential drain current while the common mode voltage at the inputs is rejected (as long as $MN3$ is switched on): the differential pair works as a differential transconductance stage. The drains of the input transistors are connected to two ideal voltage generators (V_1 and V_2). They are used to copy the current flowing through them into the two current controlled current sources (F_1 and F_2). Their output currents flow into the RC parallels ($C_1//R_1$ and $C_2//R_2$, where $R_1 = R_2 = R_{out}$ and $C_1 = C_2 = C_{out}$) raising to an amplified differential voltage $V_{dif} = R_{out} g_m V_d$; the gain of the two stages is $g_m R_{out}$ and it can be made arbitrarily high. Finally the output stage is made by the ideal voltage controlled voltage generator E_1 which converts the differential voltage into a single ended voltage and provides the low output impedance of the OpAmp.

The design of such amplifier starts with the relationship between the MOS transistor drain current and the voltages applied at its terminals:

$$I_D = \mu_n \frac{C_{OX}}{2} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \tag{2.3}$$

where μ_n is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W and L the gate width and length, V_{GS} is the voltage between the gate and the source and V_{TH} is the threshold voltage (μ_n, C_{OX} and V_{TH} are process dependent and can be considered as constants for a given technology). Such relationship does not take into account the body effect, which actually modulates the threshold voltage, and the channel length modulation: the drain current depends also on the drain to source voltage. Moreover, it is valid only if the transistor is biased in saturation, that is if $V_{DS} < V_{OD}$ where V_{OD} is the transistor overdrive voltage defined as $V_{OD} = V_{GS} - V_{TH}$.

Current mirror analysis

The current bias of the differential pair is given by the drain current provided by $MN3$ which in turn depends on the gate to source voltage set by the diode connected transistor $MN0$ of the weak side of the current mirror. Such voltage is derived by equating the current flowing trough $R0$ and the drain current of $MN0$ (no current flows in the gate of MOS transistors)

$$I_{R0} = \frac{V_{DD} - V_{GS\_MN0}}{R_0} = I_{D\_MN0} = \mu_n \frac{C_{OX}}{2} \left(\frac{W}{L}\right) (V_{GS\_MN0} - V_{TH})^2 \tag{2.4}$$

and solving the quadratic equation that follows. $V_{GS\_MN0} = V_{GS\_MN3}$, thus the drain current of $MN3$ will be a replica of the reference current $I_{REF} = I_{D\_MN0}$

scaled by the ratio between the aspect ratio of $MN0$ and $MN3$, that is:

$$I_B = I_{D\_MN3} = \frac{(W/L)_{MN3}}{(W/L)_{MN0}} I_{REf} \tag{2.5}$$

In the designed amplifier the V_{SS} terminal is connected to ground (0 V) and the positive supply voltage set by $V_{DD} = 3.3\,\mathrm{V}$. Transistors $MN0$ and $MN3$ are chosen to be with the same aspect ratio of $(W/L)_0 = (W/L)_3 = 70\,\mu\mathrm{m}/2\,\mu\mathrm{m}$, resistor $R0 = 130\,\mathrm{k}\Omega$ and the capacitor $C0 = 1\,\mathrm{pF}$ will make $MN3$ to provide an almost constant bias current of $I_B \approx 20\,\mu\mathrm{A}$.

Differential pair analysis

The operation of the differential pair is based on the matching of the input transistors, that is $(W/L)_1 = (W/L)_2$, and the assumption that they are working in saturation, so the relationship of Eqn.2.3 holds. This assumption is valid if the voltage at their gate exceeds their gate to source voltage (defined by the aspect ratio and half of the biasing current) plus the voltage headroom necessary to $MN3$ to be in saturation and also their drain to source voltage greater than the overdrive voltage (voltage at the gate lower than the voltage at the drain plus a threshold voltage). Moreover, the differential voltage should be bounded by $\pm\sqrt{2}V_{OD}$ otherwise all the bias current will flow into a single transistor and the other switches off. Within these constrains the gate to source voltages of $MN1$ and $MN2$ can be expressed as:

$$V_{GS1} = V_{TH} + \sqrt{\frac{I_{D1}}{\beta}} \qquad V_{GS2} = V_{TH} + \sqrt{\frac{I_{D2}}{\beta}} \tag{2.6}$$

where $\beta = (W/L)\mu_n C_{OX}/2$. Noting that the source of these transistors are connected together, the difference between their gate to source voltages equals also the differential voltage, i.e.

$$V_{GS1} - V_{GS2} = V_d = \sqrt{\frac{1}{\beta}}\left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right) \tag{2.7}$$

rearranging and squaring both sides

$$\beta V_d^2 = I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}} = I_B - 2\sqrt{I_{D1}I_{D2}} \tag{2.8}$$

before squaring again both sides it is worth nothing that $4I_{D1}I_{D2} = (I_{D1} + I_{D2})^2 - (I_{D1} - I_{D2})^2 = I_B^2 - (I_{D1} - I_{D2})^2$, thus

$$\left(\beta V_d^2 - I_B\right)^2 = I_B^2 - (I_{D1} - I_{D2})^2 \quad \rightarrow \quad (I_{D1} - I_{D2})^2 = 2\beta V_d^2 I_B - \beta^2 V_d^4. \tag{2.9}$$

Taking finally the square root of both sides and rearranging the right hand one, the large signal differential current expression become:

$$I_{D1} - I_{D2} = I_d = \sqrt{2\beta I_B}\ V_d\ \sqrt{1 - \frac{\beta V_d^2}{2I_B}}. \tag{2.10}$$

The gain of this differential stage is then evaluated by taking the derivative of the differential current with respect the differential voltage around the operating point, i.e. $V_d = 0\,\mathrm{V}$ leading to:

$$i_d = \sqrt{2\beta I_B}\ v_d = g_m\ v_d \tag{2.11}$$

where g_m is not only the transconductance of the stage but also the transconductance of input transistors (which are biased at $I_B/2$). In the designed amplifier the aspect ratio of $MN1$ and $MN2$ are $(W/L)_1 = (W/L)_2 = 100\,\mu\mathrm{m}/4\,\mu\mathrm{m}$ which turns into a transconductance of $g_{m1} = g_{m2} = g_m \approx 200\,\mu\mathrm{S}$.

The differential current sensed by the two voltage generators (which subtract 300 mV from the supply voltage) is forced to flow into the RC parallel providing the required high gain; the current gain of the current controlled current generators is unitary while $R_{out} = 50\,\mathrm{M}\Omega$ and $C_{out} = 30\,\mathrm{pF}$. The voltage gain of the voltage controlled voltage source is unitary, thus the low-frequency gain equals $g_m\ R_{out} \approx 80\,\mathrm{dB}$. The RC parallel is also used to set the Gain Band-Width product (GBW) of the amplifier, indeed they introduce a pole in the transfer function located at

$$f = \frac{1}{2\ \pi\ R_{out}\ C_{out}} \tag{2.12}$$

thus $GBW = g_m/(2\pi C_{out}) \approx 1\,\mathrm{MHz}$.

All the components, except the transistors of the differential pair and its biasing circuit, are ideal. The transient simulations are faster and the main characteristics of the OpAmp can be easily controlled, e.g. by varying the values of the RC parallel. Such model is well suited for the analysis of the differential stage which has been shown in literature to be responsible for the upset induced by interference applied to the amplifier's inputs.

2.2 Offset induced by RF interference

As previously mentioned, the main effect caused by the injection of CW disturbance at the amplifiers inputs is the generation of a DC offset shift in the output. Such upset was firstly analyzed by several measurement on feedback OpAmps [21]-[22]. Authors observed that the worst case is when the OpAmps were connected as voltage follower. Furthermore they found a correlation between the output DC value and the Slew Rate (SR) asymmetry; such effect is highlighted in Fig.2.4. This plot refers

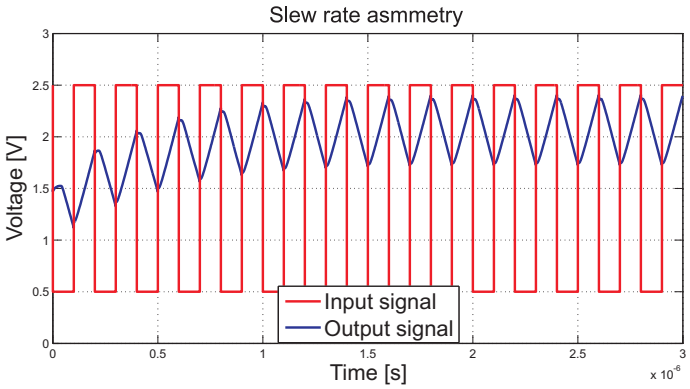


Figure 2.4: Simulation results highlighting the DC offset shift caused by the SR asymmetry.

to a simulation of the modeled OpAmp connected as voltage follower and fed by a square wave signal with frequency of 5 MHz and 1 V of amplitude.

As can be seen from the first cycles, the positive step induces an higher SR while a negative step produces the opposite effect. Such asymmetry is caused by the finite impedance of the circuit providing the bias current to the differential pair, indeed a positive input voltage step induces a higher bias current, consequently an higher SR. This unbalance causes DC offset as well, as can be seen in the last cycles, where the steady state condition is reached. It is worth nothing that this effect is a low radio-frequency effect, indeed it is assumed that the disturbance propagates trough the amplifier up to the output stage. High frequency interference are actually filtered by the transimpedance stage which follows the differential pair.

2.2.1 Model for the offset prediction

Another root cause is the disturbance rectification [23]. Authors provided also an analytical model for the offset prediction. It is assumed that the limited bandwidth of the differential input pair cuts the high-frequency disturbances before reaching the following stages. Thus, the RFIs induced offset shift is mainly due to the input stage upset. An analytical model can be derived with the series expansion of the differential drain current of Eqn.(2.10) assuming the fluctuation of both the differential voltage V_d and the bias current I_B. The DC operating point is defined by $V_d = 0\,\mathrm{V}$ and $I_B = I_0$:

$$I_d \approx I_d|_{0,I_0} + \left.\frac{\partial I_d}{\partial I_b}\right|_{0,I_0} i + \frac{1}{2}\left.\frac{\partial^2 I_d}{\partial V_d^2}\right|_{0,I_0} v_d^2 + \frac{1}{2}\left.\frac{\partial^2 I_d}{\partial I_b^2}\right|_{0,I_0} i^2 + \left.\frac{\partial^2 I_d}{\partial V_d\, I_b}\right|_{0,I_0} v_d\, i \qquad (2.13)$$

the only terms that differs from zero are the first derivative of I_d with respect to V_d and the second derivative with respect to both V_d and I_b. The former give raise to

g_m, which is the small signal gain of the stage while the latter produce a term called $g_p = \sqrt{\beta/(2I_0)}$. Equation (2.13) can be rewritten as:

$$i_d = g_m v_d + g_p v_d i. \tag{2.14}$$

v_d represents the perturbation of the differential mode input voltage and i is the fluctuation of the bias current.

In the case of a simultaneous fluctuation of the differential voltage $V_p cos(\omega t + \phi_v)$ together with the bias current $I_p cos(\omega t + \phi_i)$, Eqn.(2.14) reads:

$$\begin{aligned} i_d(t) &= g_m V_p cos(\omega t + \phi_v) + g_p V_p cos(\omega t + \phi_v) I_p cos(\omega t + \phi_i) \\ &= g_m V_p cos(\omega t + \phi_v) + \frac{g_p V_p I_p}{2}\Big(cos(\phi_v - \phi_i) + cos(2\omega t + \phi_v + \phi_i)\Big) \end{aligned}$$

having average (DC magnitude) equal to:

$$\Delta I_d = \frac{g_p V_p I_p}{2} cos(\phi_v - \phi_i) \tag{2.15}$$

and the input referred offset is readily calculated as:

$$\Delta V_{off} = \frac{\Delta I_d}{g_m}. \tag{2.16}$$

Bias current fluctuation

The effective bias current fluctuation can be evaluated from the small signal analysis of the differential pair referring to the equivalent circuit is depicted in Fig.2.5 and assuming $g_{m1} = g_{m2} = g_m$ and $C_{gs1} = C_{gs2} = C_{gs}$. The tail current, see appendix

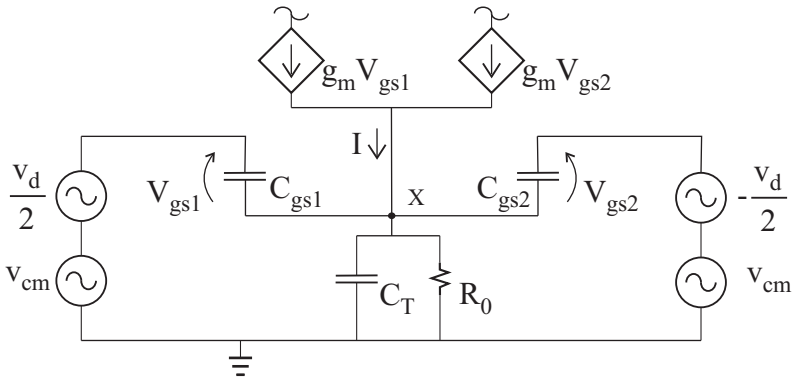


Figure 2.5: Differential pair small-signal equivalent circuit.

A.1, can be expressed as:

$$I(j\omega) = \frac{2g_m(j\omega\ C_T\ R_0 + 1)}{j\omega\ (2C_{gs} + C_T)\ R_0 + 2g_m\ R_0 + 1} V_{cm}(j\omega) = Y(j\omega)\ V_{cm}(j\omega) \tag{2.17}$$

where R_0 is the current mirror output resistance and C_T is the parasitic capacitance between the common source node and ground. The differential mode contribution cancel out and the bias current fluctuation shows dependance only on the common mode component of the input voltage. Performing the inverse Fourier transform of both the differential voltage and of the bias current of Eqn.(2.17) it is possible to derive a time-domain expression of the offset voltage depending only on the differential and common mode voltages at the inputs of the OpAmp.

Voltage follower analysis

Referring to the designed amplifier of Fig.2.3, the open-loop differential gain is derived:

$$A_d(j\omega) = \frac{V_{OUT}}{V_+ - V_-} = \frac{g_m\ R_{out}}{1 + j\omega R_{out}\ C_{out}}. \tag{2.18}$$

where R_{out} and C_{out} constitutes the RC parallel which loads the transimpedance stage. They are used to control the amplifier's low-frequency gain and the dominating pole (see Eqn. 2.12). The output voltage of the OpAmp connected as voltage follower, considering the finite gain and the bandwidth, leads to the following expression:

$$V_{OUT} = V_- = \frac{A_d}{1 + A_d} V_+(j\omega) \tag{2.19}$$

The differential mode V_d and common mode V_{cm} components of the input are thus derived to be:

$$V_d(j\omega) = \frac{V_+}{(1\ +\ A_d)} = K_d(j\omega)\ V_+(j\omega) \tag{2.20}$$

$$V_{cm}(j\omega) = \frac{V_+}{2}\left(\frac{1\ +2\ A_d}{1\ +\ A_d}\right) = K_{cm}(j\omega)\ V_+(j\omega) \tag{2.21}$$

The time domain expressions of the differential mode $v_d(t)$ and common mode $v_{cm}(t)$ voltages are derived supposing a CW interference expressed as $V_+(t) = V_p cos(\omega_1 t)$ injected at the non-inverting input and performing the inverse Fourier Transform of (2.20) and (2.21):

$$v_d(t) = \mathcal{F}^{-1}[V_d(j\omega_1)] = |K_d(j\omega_1)|\ V_p cos\Big(\omega_1 t + \angle K_d(j\omega_1)\Big) \tag{2.22}$$

$$v_{cm}(t) = \mathcal{F}^{-1}[V_{cm}(j\omega_1)] = |K_{cm}(j\omega_1)|\ V_p cos\Big(\omega_1 t + \angle K_{cm}(j\omega_1)\Big) \tag{2.23}$$

The differential drain current is thus evaluated substituting $v_d(t)$ and $v_{cm}(t)$ in (2.14):

$$\begin{aligned} i_d(t) = {} & g_m|K_d(j\omega_1)|\ V_p cos\Big(\omega_1 t + \angle K_d(j\omega_1)\Big) + \\ & + g_p|K_d(j\omega_1)|\ V_p cos\Big(\omega_1 t + \angle K_d(j\omega_1)\Big) \times |I(j\omega)|\ cos\Big(\omega_1 t + \angle I(j\omega_1)\Big) \end{aligned} \quad (2.24)$$

and the EMI induced offset is calculated dividing the DC component of the differential current (ΔI_d) by the transconductance of the stage, Eqn.(2.16). The first term of (2.24) has no DC component; it is a constant term multiplied by a time shifted sinusoid. The two *cos* product can be rewritten as:

$$cos\Big(\omega t + \phi_1\Big)cos\Big(\omega t + \phi_2\Big) = \frac{cos\Big(\phi_1 - \phi_2\Big)}{2} + \frac{cos\Big(2\omega t + \phi_1 + \phi_2\Big)}{2} \quad (2.25)$$

where the first term in the right hand side is responsible for the DC offset. It can be rewritten as:

$$\begin{aligned} \Delta V_{off} = \frac{\Delta I_d}{g_m} = \frac{g_p V_p\ |K_d|\ |I| cos\Big(\angle I - \angle K_d\Big)}{2\ g_m} = \\ = \frac{g_p\ |K_d|\ |Y\ K_{cm}|\ V_p^2 cos\Big(\angle Y K_{cm} - \angle K_d\Big)}{2\ g_m} \end{aligned}$$

where $Y(j\omega)$ is the admittance relating the bias current fluctuation to the common mode component of the input voltage, see Eqn.(2.17).

Simulation results for the RFI induced offset

The RFIs induced offset is also simulated by connecting the OpAmp model of Fig.2.3 as a voltage follower and applying the interference (with a sinusoidal voltage generator) directly at the non-inverting input. The analysis performed is a parametric transient simulation varying both the interference frequency (from 2 MHz to 1 GHz) and peak voltage ($RFampl$). The stop time is set to hundreds of the interference cycles since the steady state condition has to be reached. The worst case in terms of simulation stop time (that is the slower response with respect to the interference period) is observed at the higher frequency and for higher amplitudes (1500 period for the interference frequency of 1 GHz and $RFampl = 500$ mV). The DC voltage offset referred to the input is actually the offset appearing at the output node. It is calculated by clipping the output waveform in the last 50 periods and averaging; then the DC value of the inverting input is subtracted (the finite gain introduces offset as well).

The validity of the model has been verified by increasing the amplitude of the interference. In Fig.2.6 it is lower than the input transistor overdrive voltage ($V_{OD} \approx$

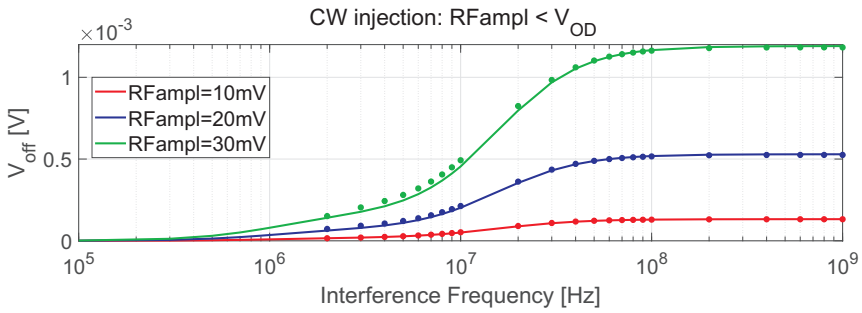


Figure 2.6: Simulation of EMI induced offset due to CW injection (RF amplitude lower than the overdrive voltage).

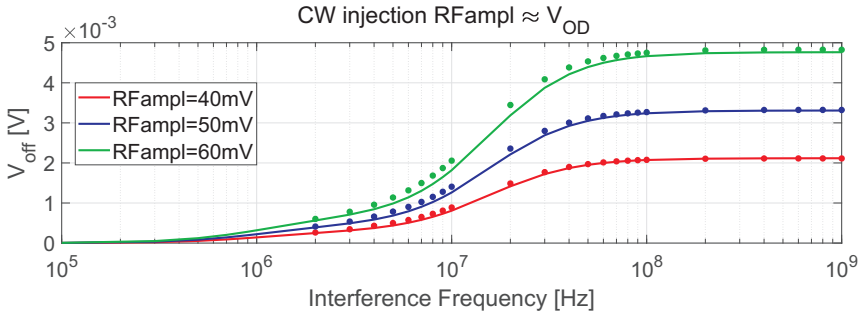


Figure 2.7: Simulation of EMI induced offset due to CW injection (RF amplitude near the overdrive voltage).

55 mV). The modeled offset (continuous line) matches well the simulation results (stars) throughout the frequency range of interest. In the next set of simulations, the interference amplitude is further increased. As can be seen from Fig.2.7, the model can still be used in the case of continuous wave interference having $RFampl \approx V_{OD}$. The modeled offset (continuous line) actually underestimates the simulated one (stars) in the lower frequency range (interference frequency less than 50 MHz).

If the amplitude of the disturbance is higher than the input transistor overdrive voltage, the device is periodically brought out of the saturation region and switched off [24]. The square relationship between the drain current and the gate to source voltage is no longer valid for each instant of time and the analytical model deviates from simulation results. It can be seen clearly in Fig.2.8(a), (b) where the model underestimates the simulated offset. The model does not provide any useful offset estimation, see Fig.2.8(c), in the case of an injected interference with amplitude $RFampl = 500\,\text{mV} \gg V_{OD}$.

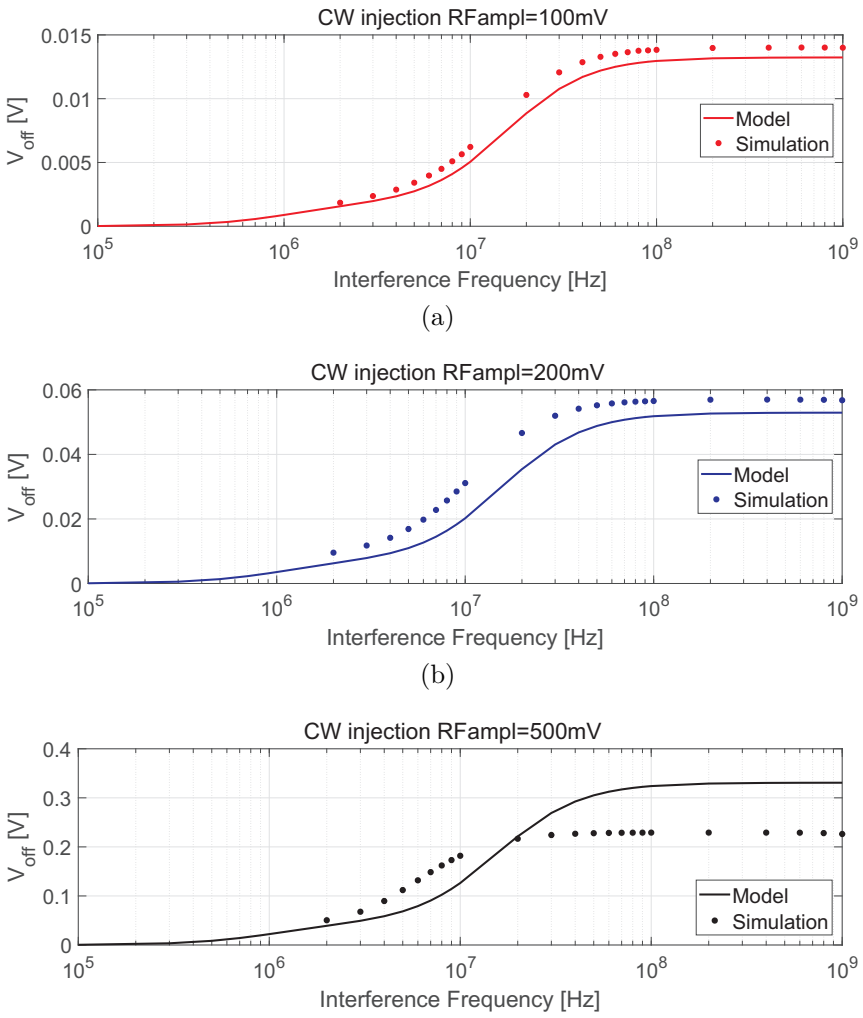


Figure 2.8: Simulation of EMI induced offset due to CW injection (RF amplitude higher than the overdrive voltage).

2.3 Measurement and evaluation of the EMI susceptibility

The IEC-62132 deals with the measurement of the conducted and radiated susceptibility of ICs to conducted and radiated disturbance in the 150 kHz-1 GHz frequency range. In particular, the part 4 [26] describes the measurement method to evaluate the susceptibility of ICs to conducted RF disturbance. This method, also known as Direct RF Power Injection is guaranteed to have a high degree of repeatability and correlation of immunity measurements. It basically requires the DPI test board,

i.e. a proper Printed Circuit Board (PCB), the RF injection circuit and the IC monitoring.

The ICs susceptibility, during the DPI testing, can be predicted by computer simulations; test benches, however, must comprise at least electrical models of the injection setup and of the test board [30]. Moreover, modern integrated circuits enclose several blocks within the same package. In a smart power switch, for example, the digital core, the front-end analog circuits, the driver and the power transistor can be embedded together. The simulation of a single susceptible block requires then the modelling of package interconnects, other blocks and the substrate [31]: RFI injected at a single port, indeed, spreads among all of them.

2.3.1 DPI set-up

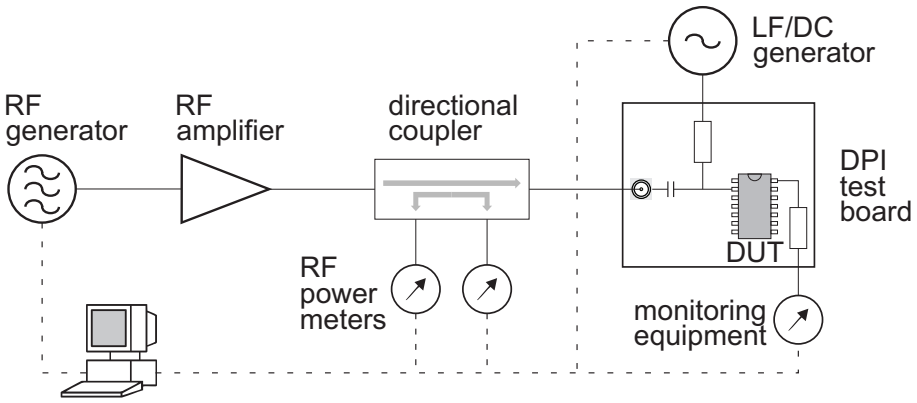


Figure 2.9: DPI test set-up.

The test setup for the Direct RF Power Injection Method is depicted in Fig.2.9. From left to right there is the RF generator which has to provide the interference signal with frequency from 150 kHz to 1 GHz (linear or logarithmic steps counting $\approx$ 200 frequency points as specified in IEC 62132-1 [32]). Such disturbance can be a Continuous Wave and/or and Amplitude Modulated (AM) signal. By default, the modulated signal has frequency of 1 kHz and the modulation depth is 80%. For each frequency point the interference is injected at constant power for the time (dwell time) necessary to the DUT to respond to the disturbance. The injected power is then increased until the malfunction (susceptibility criterion) has been registered or the maximum power level reached. Such procedure is repeated for all the pins for which the test is required.

The RF amplifier and the directional coupler are used to amplify and to check the power level at the injection point. Indeed, the power meters at the coupled ports read the forward and the reflected power of the signal that is injected. The

maximum injected power depends on protective zones, e.g. for unprotected device such as high side switches or power supply circuits (zone 1) the maximum injected power is 37 dBm (≈ 5 W). Signal conditioning devices are usually protected by low-pass filters and the maximum power to be injected shall be 27 dBm (≈ 0.5 mW). If the AM signal is used, then the peak power shall be the same as for the CW counterpart.

Interference at the injection point shall be decoupled from supply or input signal generators (LF/DC generator in figure) via a DC blocking capacitor and decoupling network (also a Bias Tee can be used for the same purpose). Finally the output of interest shall be decoupled, to avoid crosstalk, and monitored. Such closed-loop test set-up can be controlled by a computer and the procedure automated.

The advantage of using such measurement technique is not only the high reproducibility of the measured susceptibility-profile but also the possibility of deriving the interference reaching the input of the DUT, thus translating the DPI specification at the PCB level to pin level. It can be accomplished by the model of the injection path (from the 50 Ω RF amplifier up to the decoupling capacitor) and of the PCB test board. It can be evaluated by the equivalent circuit extraction from the frequency characteristic measurement.

2.3.2 Model for DPI analysis

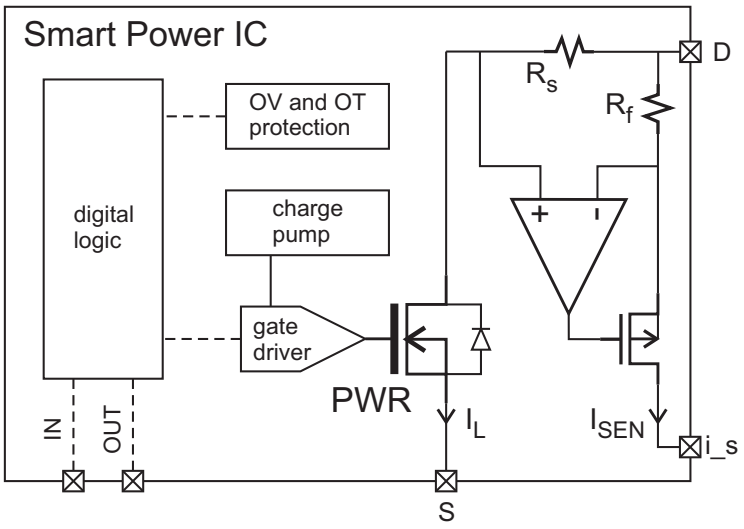


Figure 2.10: Block diagram of the Smart Power IC.

In this subsection, the propagation of interference from the DPI injection point to the inputs of a susceptible subcircuit is presented. The device under test, sketched in Fig.2.10, is a smart high-side power switch which incorporates two dies: the

power MOS (PWR) and its driver (DRV), both of them are enclosed in a plastic package. DRV comprises several analog and digital subcircuits: the current sensor (highlighted in the right), the PWR gate driver, the charge pump, the over-voltage and over-temperature protections and the digital core. An electrical model (MOD hereinafter) of the entire structure is developed with the aim of deriving the magnitude of the interference reaching each subcircuit and to identify the more susceptible ones. In particular the macromodel has been used to setup simulations aimed to analyze the susceptibility of the amplifier used as current sensor and compare the upset with the DPI test results.

One application of OpAmps used as building block in the analog front-end circuits embedded within ICs is provided in Fig.2.10. In this case, the amplifier is used for the high-side current sensing. Basically, the high-gain and the feedback force the voltage drop across R_s and R_f to be the same, thus the current I_{SEN} results to be proportional to the load current I_L and the resistors ratio. The advantages of this technique are the detection of the high current caused by accidental shorts and the direct connection of the load to the system ground. The disadvantages are the high common mode voltage to which the OpAmp is subjected and the need of high voltage devices, therefore a more complex design and an higher cost. Another disadvantage regarding the EMC issue is that power-supply circuits must withstand to the highest injected power of 37 dBm.

Proposed method

The proposed method is useful for the evaluation of the susceptibility of a subcircuit included in a complex integrated circuit during the DPI test. The first step is the identification of the injection point at the PCB level, usually the SMA connector, and the modeling of the injection path between such point and the package terminals (INJ MOD). Afterwards the package (PKG MOD) and each IC encapsulated in it has to be modeled (PWR MOD and DRV MOD on the right of Fig.2.11). The macromodel is then build up by connecting together all the extracted equivalent blocks and the cell under investigation can thus be analyzed performing computer simulations. The whole macromodel is shown in Fig.2.11.

The influence of the PCB and the decoupling networks between the interference injection point and each IC's pin has been derived from the scattering measurements performed on the test board itself. The traces between the injection ports and the decoupling networks were made much shorter than the shortest electrical length involved in the measurements ($< \lambda_{1\,\mathrm{GHz}}/20$, where $\lambda_{1\,\mathrm{GHz}} = 30\,\mathrm{cm}$). The contribution of these transmission lines, therefore, was considered negligible and not included in the equivalent circuits (fitted directly from S-parameters).

The equivalent circuit of the RFI injection path from the SMA connector to the D pin (essentially the bias tee and the power-supply decoupling capacitor) is

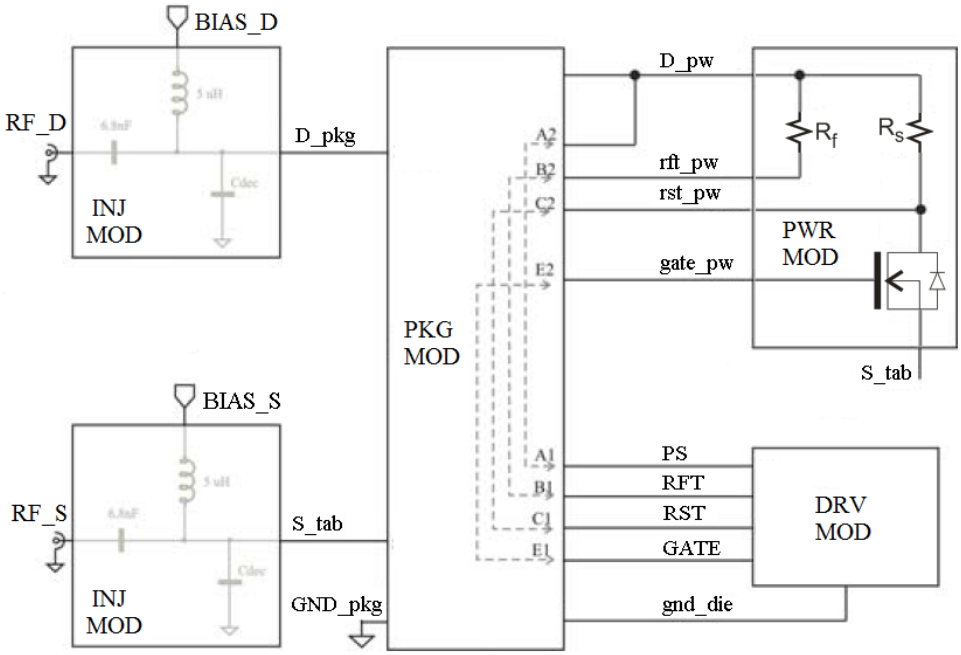


Figure 2.11: Macromodel of the Smart Power IC used for the DPI analysis.

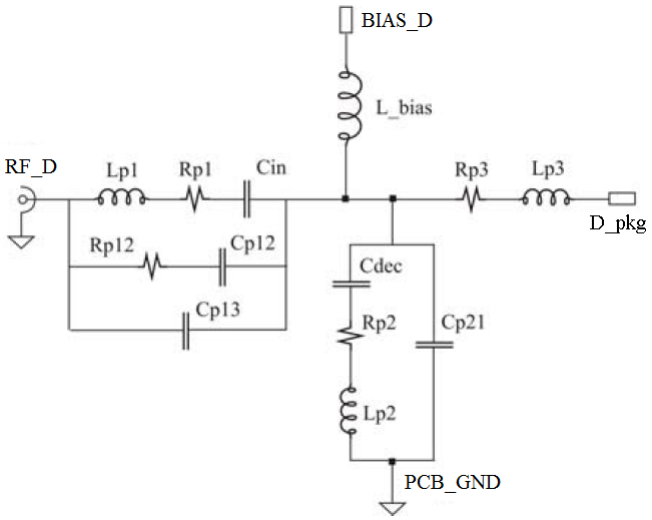


Figure 2.12: Equivalent circuit of the injection path from SMA to the D pin (extracted from measurements).

provided in Fig.2.12 as an example. A similar circuit is derived for the injection path at the S pin.

The equivalent circuit used to model the package (PKG MOD), on the other

hand, has been extracted from finite-element method simulations (Ansys Q3D Extractor).

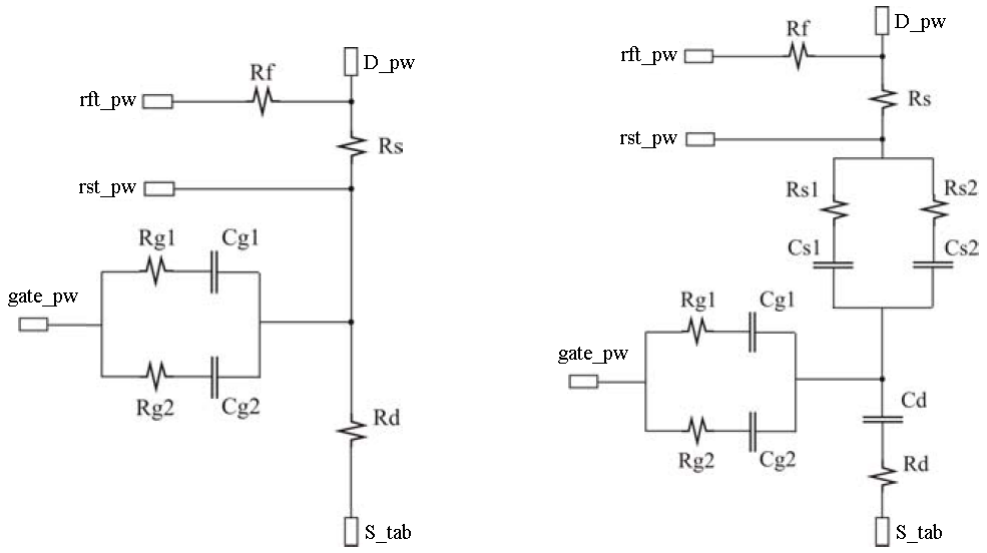


Figure 2.13: Equivalent circuit of the power MOS switched ON (a) and OFF (b) extracted from measurements.

Injected interference usually propagates through the lower-impedance path, therefore the supply rail, the power MOS but also the substrate should be modeled carefully. To this purpose the power MOS has been placed on a proper test board and a set of 2-port scattering parameter measurements have been performed by a network analyzer connected to two (Ground-Signal) G-S microprobes. The instrument and the probes were calibrated with the short-open-load-thru calibration kit (Picoprobe Calibration Substrate CS-5). The test fixture was then de-embedded from measurement results. In this way the reference plane has been moved from the instrument outputs to the tips of the probes. The extracted equivalent circuits of the transistor switched ON and OFF are shown in Fig.2.13(a) and Fig.2.13(b) respectively.

The same method has been used to obtain the model of the DRV chip: a sample has been placed on a top-on-carrier and properly layouted to contact, with the G-S RF microprobes, the input pads (which are bonded to the die pads). The measured scattering parameters were then fitted to obtain the equivalent circuit of Fig.2.14.

Comparison between simulation and measurements results

The macromodel depicted in Fig.2.11 has been obtained by connecting the above-mentioned equivalent blocks. It has been simulated to derive the magnitude of the

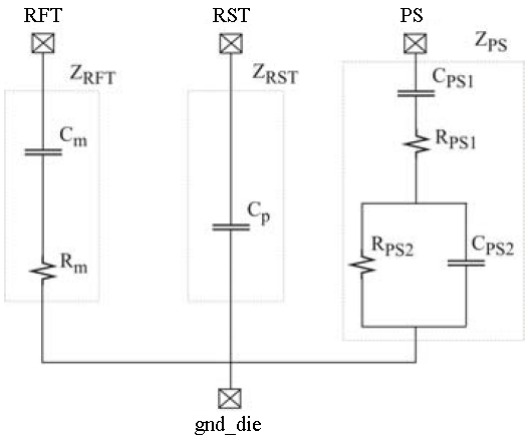


Figure 2.14: Equivalent circuit of the top chip extracted from measurements.

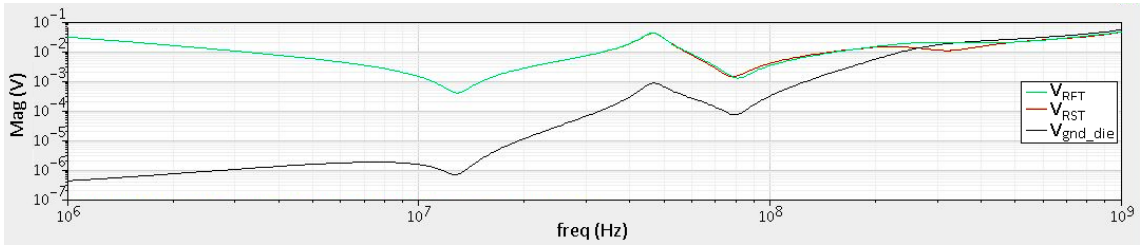
interference at the amplifier's inputs as shown in Fig.2.15, and thus to investigate its susceptibility to the injected RF interference. A 50 Ω RF source is connected at the RF_D input to simulate the injection in the power-supply rail and an AC analysis is performed probing the input voltages of the amplifier under analysis, i.e. *RFT*, *RST* and *gnd_die* as showed in Fig.2.15(a) in green, brown and black respectively. The differential mode V_{dm} and the common mode V_{cm} component are expressed as:

$$V_d = V_{RFT} - V_{RST} \tag{2.26}$$

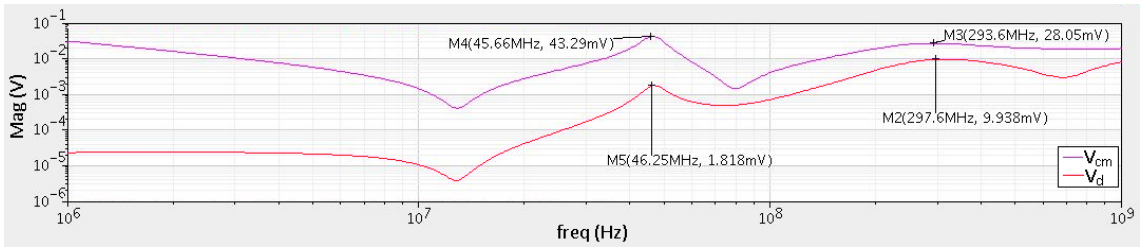
$$V_{cm} = \frac{1}{2}\Big((V_{RFT} - V_{gnd\_die}) + (V_{RST} - V_{gnd\_die})\Big). \tag{2.27}$$

Both are plotted in Fig.2.15(b) in red and magenta. In the graph of Fig.2.15 (c), there is the product of the two components versus the frequency. This last plot is of particular interest, indeed it has been shown in literature that the offset induced by RFIs applied at the input of OpAmps is dependent on the product of the common-mode voltage and differential-mode voltage [23]. Such DC offset voltage is applied to the output transistor's gate, thus translated in a DC current shift leading to an upset in the sensed current I_{SEN} (the OpAmp is working as a transconductance amplifier).

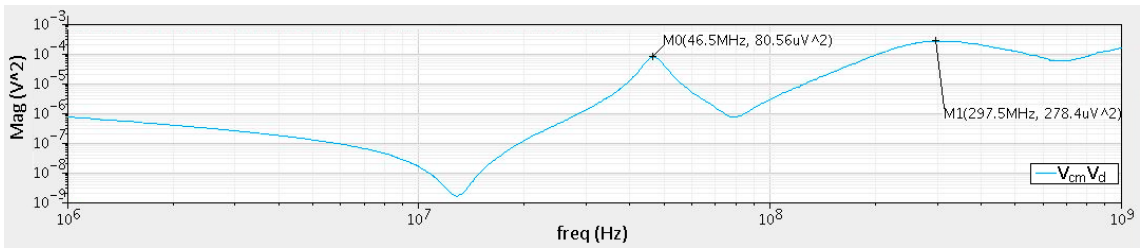
Referring to simulation results, there are two maximums in the product of the common-mode and differential mode voltages, the first around 45 MHz, while the second at about 300 MHz, therefore the worst case condition is supposed to be when the injected disturbance has frequency around those two. The macromodel has been also used to derive the magnitude of such voltage components for three power levels of the RFI injected at the PCB level, as shown in Table 2.1. These data are useful to perform simulations for the analysis of the OpAmp subjected to the actual interference coming from the injection of RFIs during the DPI test. Time domain



(a)



(b)



(c)

Figure 2.15: Macromodel AC simulation for the amplifier susceptibility analysis (PWR switched OFF). Probed voltages (a), common mode and differential mode (b) and their product (c).

simulation can be performed either on the cell under analysis alone and equivalent RF sources or by properly connecting the circuit to the macromodel.

Finally the susceptibility of the smart-power switch has been evaluated performing the DPI test. The complete device is soldered on the test board and the average value of the current sensor's output is monitored while RFIs are injected into each pin. Test results for the injection into the power supply line (RF_D terminal) with the power transistor switched off are shown in Fig.2.16. The maximum of the susceptibility of the current sensor is around the two predicted frequencies, i.e. 45 MHz and 300 MHz.

Inj into RF_D		f=45 MHz		f=300 MHz	
P_{inj} [dBm]	$\|V_{RF}\|$ [V]	$\|V_d\|$ [mV]	$\|V_{cm}\|$ [mV]	$\|V_d\|$ [mV]	$\|V_{cm}\|$ [mV]
4	1	2.86	45.37	11.86	27.2
20	6	17	272	71	163
30	20	57	907	237	544

Table 2.1: Magnitude of the common-mode and differential-mode voltages (injection in RF_D)

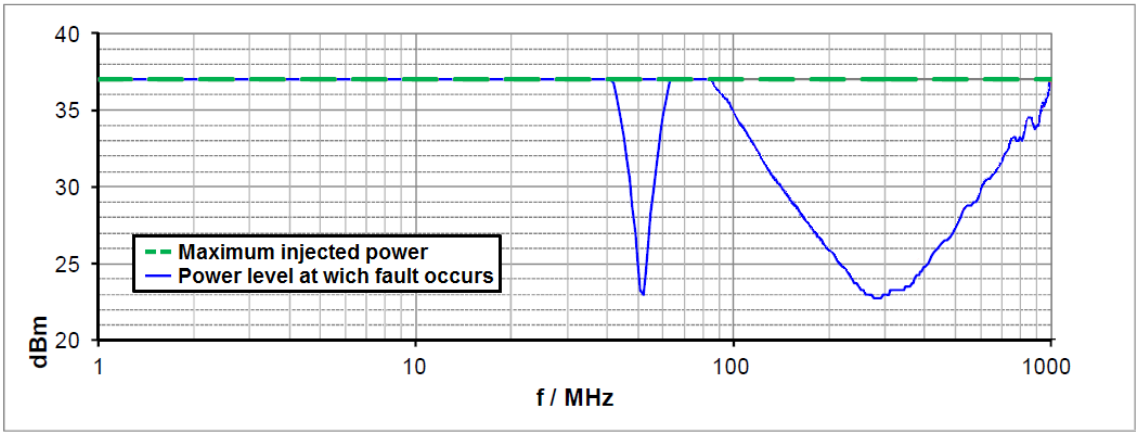


Figure 2.16: DPI test results (PWR switched OFF).

Discussion

An effective method to model complex ICs and to evaluate subcircuit susceptibility to EMC by means of simulations has been shown. The equivalent circuits representing the injection path at the PCB level and the two dies encapsulated in the package were extracted from the fitting of S-parameter measurements. The model of the package itself has been derived from FEM simulations. The macromodel obtained connecting electrically-equivalent blocks has been used to analyze a particular subcircuit within the IC, that is an amplifier used for the high-side current sensing. The simulations predicted two frequency bands in which the amplifier has higher probability of being susceptible to the injected disturbance. The DPI test results confirmed such prediction. It not only validates the proposed macromodeling

technique but also the assumption that the maximum product of the common-mode and differential-mode voltages at the amplifier's inputs would induce the higher susceptibility.

Chapter 3

Investigation on the EMIRR to qualify OpAmps

In the particular case of OpAmps, the upset induced by the injection of CW signal into its input terminals is the generation of a DC offset shift in the output. A metric based on this susceptibility criterion, namely the EMI Rejection Ratio (EMIRR), has been introduced by Texas Instrument with the aim of characterizing the immunity of OpAmps to RFIs [33]. This metric has been adopted also by other manufacturers appearing in datasheets [34]-[35] as a figure of merit in the selection of OpAmps. An EMI robust IC, indeed, will led to a robust equipment once embedded in it. As a consequence, this equipment will be more prone to be compliant to the EMC directives.

The EMIRR is evaluated injecting a small-amplitude RF signal into the OpAmp inputs and measuring the resulting DC offset shift at the output. The test that has to be performed is similar to the DPI method; basically, this measurement technique is used to derive the lowest-power CW-interference leading the IC under test to a specified malfunctions. The test setup for the EMIRR evaluation uses the amplitude of the injected CW interference rather then the forward power and it is assumed that the RFI induced offset is in quadratic relationship with it. This assumption has been shown in Section 3.1.1 to be true only for low-amplitude interfering signals. It limited, de facto, the usefulness of the EMIRR in qualifying the response of OpAmps to low-power interfering signals only. In Section 3.2, this has also been proven by measurements on several commercially-available OpAmps.

3.1 EMI Rejection Ratio

Texas Instruments in the application reports [36] and [37] introduced the EMIRR to qualify the immunity of operational amplifiers to electromagnetic disturbance. This

parameter is based on the measurement of the DC offset shift (ΔV_{off}) induced by the injection of a CW radio frequency interference into the input of OpAmps. The EMIRR is defined as follows

$$\text{EMIRR} = 20\ log_{10}\left(\frac{V_p}{\Delta V_{\text{off}}}\right) + 20\ log_{10}\left(\frac{V_p}{100\,\text{mV}}\right). \tag{3.1}$$

Where V_p is the peak amplitude of the disturbance at the injection point, i.e., the pin of the Device Under Test (DUT). The standard measurement condition of $V_p = 100\,\text{mV}$ is used for normalization as in [36]. Once the DC offset shift is measured and EMIRR evaluated, it is possible to derive the offset voltage for any interference by the following equation:

$$\Delta V_{off} = \left(\frac{{V_p}^2}{100\,\text{mV}}\right) 10^{-\left(\frac{EMIRR}{20}\right)}. \tag{3.2}$$

Based on the EMIRR definition, the EMI induced offset is proportional to the square of V_p. Such relation has been shown hereinafter to be valid only under some assumptions, mainly the weak non-linearity (kind of small-signal assumption). It makes the EMIRR, as the name itself suggests, a small-signal parameter not suitable for predicting the offset in the case of high-amplitude RFIs applied to the OpAmp's inputs.

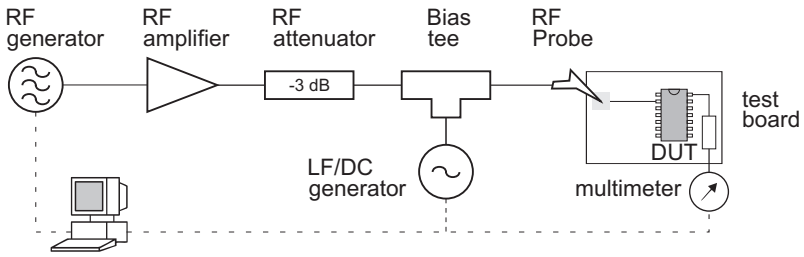


Figure 3.1: Measurement test set-up for the EMIRR and the offset evaluations.

The EMIRR measurement requires to inject a well defined EMI and the monitoring of the voltage offset shift at the amplifier's output. The disturbance amplitude at the amplifier's input can be derived by allowing a single voltage reflection. The OpAmp input impedance, indeed, is usually mismatched from the system $50\,\Omega$ but can be measured with a network analyzer. The test setup arrangement used for the EMIRR evaluation and the offset measurement is depicted in Fig.3.1.

Radio frequency CW interference coming from the RF generator (Agilent E8257D) are amplified through the RF amplifier (Amplifier Research 10W1000B) and then attenuated. The $-3\,\text{dB}$ RF attenuator (Bird Technologies 50-A-MFN-03) is used

to protected the RF amplifier from being damaged by the reflected power. The resulting disturbance is then applied to the Bias Tee (Aeroflex Inmet 8800NMF2-06) which sums interference with the DUT bias voltage provided by the LF/DC generator (Agilent 33120A Function/Arbitrary Waveform Generator). This signal reaches the OpAmp's input pad through the RF probe (Cascade Microtech P-04-N3S-SG-1270 |Z| probe) contact. The output is monitored by the multimeter (Agilent 34401A 6 1/2 Digit Multimeter) and the offset ($\Delta V_{\text{off}} = V_{\text{out\_RFI\_on}} - V_{\text{out\_RFI\_off}}$) is calculated as the difference between the OpAmp DC output voltage with the RF signal switched on and off respectively. RFIs are injected at a constant power (calibrated before the injection and checked after) of $-15\,\text{dBm}$, $-10\,\text{dBm}$, $0\,\text{dBm}$, $5\,\text{dBm}$ and $10\,\text{dBm}$; the frequency of the disturbance ranges from $10\,\text{MHz}$ to $1\,\text{GHz}$.

3.1.1 Quadratic relationship between offset and RFI peak amplitude

The square relationship between the input referred offset ΔV_{off} and the square of the peak amplitude V_p of the applied disturbance can be derived referring to the circuit of Fig.3.2. It represents the differential pair, i.e. the most used analog block for the OpAmp input stage. The analysis is based on the assumption that the CMOS input transistors M_p and M_m are biased in saturation. The same analysis can be carried out on the bipolar counterpart.

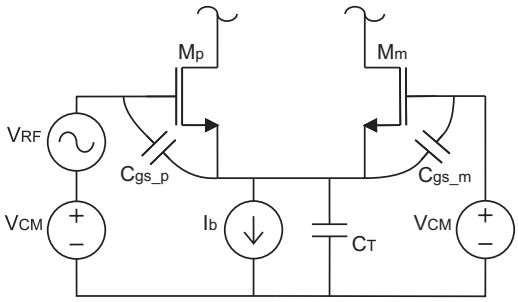


Figure 3.2: Differential pair schematic.

In the case of RFI injected in the input of an OpAmp connected as voltage follower, the output experiences a DC voltage offset and a small amplitude distorted sinusoidal signal [22]. For this reason the inverting input (gate of M_m) can be considered at a constant DC voltage (V_{CM}), within the common mode input range. All the transistors, thus, are biased in saturation. The disturbance V_{RF} is applied to the non-inverting input transistor M_p only. The small-signal analysis of the equivalent circuit of the schematic of Fig.3.2 is derived in appendix A.2. It leads to the following expressions for the gate to source voltage of M_p ($V_{\text{gs\_p}}$) and of M_m

($V_{\mathrm{gs\_m}}$):

$$V_{\mathrm{gs\_p}}(j\omega) = \frac{g_m + j\omega[C_T + C_{\mathrm{gs}}]}{2g_m + j\omega[C_T + 2C_{\mathrm{gs}}]} V_{\mathrm{RF}}(j\omega) \tag{3.3}$$

$$V_{\mathrm{gs\_m}}(j\omega) = -\frac{g_m + j\omega C_{\mathrm{gs}}}{2g_m + j\omega[C_T + 2C_{\mathrm{gs}}]} V_{\mathrm{RF}}(j\omega) \tag{3.4}$$

where the transconductance of the two input transistor and their gate to source parasitic capacitances are assumed to be equal ($g_m = g_{\mathrm{m\_p}} = g_{\mathrm{m\_m}}$ and $C_{\mathrm{gs}} = C_{\mathrm{gs\_p}} = C_{\mathrm{gs\_m}}$). C_T is the parasitic capacitance between the common source node and ground. Equations 3.4 can be rewritten directly in time domain [24]:

$$V_{\mathrm{gs\_p}}(t) = \frac{C_T + C_{\mathrm{gs}}}{C_T + 2C_{\mathrm{gs}}} V_{\mathrm{RF}}(t) \tag{3.5}$$

$$V_{\mathrm{gs\_m}}(t) = -\frac{C_{\mathrm{gs}}}{C_T + 2C_{\mathrm{gs}}} V_{\mathrm{RF}}(t). \tag{3.6}$$

The input referred offset shift ΔV_{off} can be calculated estimating the difference between the mean drain current of M_p and M_m and dividing the result by the transconductance of the differential stage. The two mean current are evaluated integrating the drain current over one interference period $T = 1/f_d$:

$$\overline{i_D} = \frac{1}{T}\int_0^T \mu_n \frac{C_{\mathrm{OX}}}{2}\left(\frac{W}{L}\right)\left[V_{\mathrm{GS}} + V_{\mathrm{gs}}(t) - V_{\mathrm{TH}}\right]^2 dt \tag{3.7}$$

The mean value of the drain currents, representing the CW radio frequency interference as $V_{\mathrm{RF}}(t) = V_p \cos(2\pi f_d t)$, become:

$$\overline{i_{D\_p}} = \beta_n (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 + \beta_n \frac{V_p^2}{2}\left(\frac{C_T + C_{\mathrm{gs}}}{C_T + 2C_{\mathrm{gs}}}\right)^2 \tag{3.8}$$

$$\overline{i_{D\_m}} = \beta_n (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 + \beta_n \frac{V_p^2}{2}\left(\frac{C_{\mathrm{gs}}}{C_T + 2C_{\mathrm{gs}}}\right)^2. \tag{3.9}$$

The first term in the right hand side of Equations 3.9 is equal to half the bias current. The second is the disturbance induced upset in the drain currents. Finally ΔV_{off} turns into:

$$\Delta V_{\mathrm{off}} = \frac{\Delta\overline{i_D}}{g_m} = \frac{V_p^2}{2(V_{\mathrm{GS}} - V_{\mathrm{TH}})}\left(\frac{C_T^2 + 2C_T C_{\mathrm{gs}}}{(C_T + 2C_{\mathrm{gs}})^2}\right). \tag{3.10}$$

This relationship is valid only for MOS transistors biased in saturation, under the assumptions of high-frequency low-amplitude CW interference. Higher-amplitude disturbances lead the input transistor to be switched off periodically. This phenomenon take place when

$$V_{\mathrm{GS}} + V_{\mathrm{gs}}(t) \leq V_{\mathrm{TH}} \tag{3.11}$$

i.e., $V_{\mathrm{gs}}(t) \geq V_{\mathrm{GS}} - V_{\mathrm{TH}}$. In this case the DC drain current shifts experienced by the input transistors cannot be described by Eqn.(3.9), and (3.10) is no longer valid. To get the actual offset the mean value of the transistors drain current has to be calculated considering also the time interval in which M_p and M_m are switched off [24].

If we consider the differential pair of Fig.3.2 composed of Bipolar Junction Transistors (BJTs), the small signal analysis lead to the same results if we substitute the gate to source voltage with the base emitter voltage and the gate-source parasitic capacitance with the base-emitter parasitic capacitance, usually indicated as C_π). The mean collector current become:

$$\overline{i_C} = \frac{1}{T}\int_0^T I_S \exp\left(\frac{V_{\mathrm{BE}} + V_{\mathrm{be}}(t)}{V_T}\right) \tag{3.12}$$

where I_S is the reverse saturation current, V_{BE} is the base emitter voltage defined by the transistor operating point, V_{be} its time varying component and V_T the thermal voltage. Substituting the exponential with its series expansion truncated to the second order, that is $\exp(x) = 1 + x + x^2/2$, we come to an expression in which the offset is in a quadratic relationship with V_p.

$$\Delta V_{\mathrm{off}} = \frac{\Delta\overline{i_C}}{g_m} = \frac{V_p^2}{4V_T}\left(\frac{C_T^2 + 2C_T C_{\mathrm{be}}}{(C_T + 2C_{\mathrm{be}})^2}\right) \tag{3.13}$$

The only assumption to be taken (according to [18]) is the small peak amplitude, thus $V_{\mathrm{be}}(t) < V_T$. A more realistic solution of the integral involves the Modified Bessel function of the first kind of zero order [38].

In conclusion the quadratic relationship between the RFIs induced offset and the disturbance amplitude of (3.10) and (3.13), are valid only for small amplitude disturbances, i.e. gate to source voltage time varying component should be lower than the overdrive voltage of the input MOSFETs and the base-emitter voltage of the input BJTs lower than the thermal voltage.

$$V_{gs}(t) < (V_{GS} - V_{TH}) \qquad V_{be}(t) < V_T. \tag{3.14}$$

3.2 EMIRR evaluation on commercially available OpAmps

Several commercially available OpAmps from different producers were tested for the EMIRR investigation; as can be seen from the list reported in Table 3.1, both the Bipolar and the CMOS technologies were taken under consideration.

All the OpAmps were soldered on a test PCB and connected as voltage followers as depicted in figure 3.3. There were two $0\,\Omega$ resistors: one between the inverting

Part name	Short description	Producer	Technology
OPA2277	High-precision OpAmp		Bipolar
OPA2333	Micro-Power, High-precision OpAmp		CMOS
TSZ122	Very high accuracy, zero drift, micropower Op Amp		CMOS
MCP6V02	Auto-Zeroed OpAmp		CMOS

Table 3.1: OpAmps used for the EMIRR investigation.

input and the output (R_{FB}) and the other in series with the non-inverting input (R_S). The output load was a capacitor (C_{OUT}): it has been used to filter interference and a high capacitance was preferable. The chosen output capacitor for the OPA2277 and the TSZ122 was of 220 pF. This output capacitance has been reduced to 100 pF for the OPA2333 and the MCP6V02 to avoid stability problems. The circuit was completed with two decoupling capacitors of 100 nF between the positive supply pin (V_{DD}) and the ground, and between the negative supply pin (V_{SS}) and the ground (C_{DD} and C_{SS} respectively). OpAmps are supplied with a symmetric voltage of ± 2.5 V and the non-inverting input (IN) is kept at a constant DC voltage of 0 V (in the middle of the common mode input range).

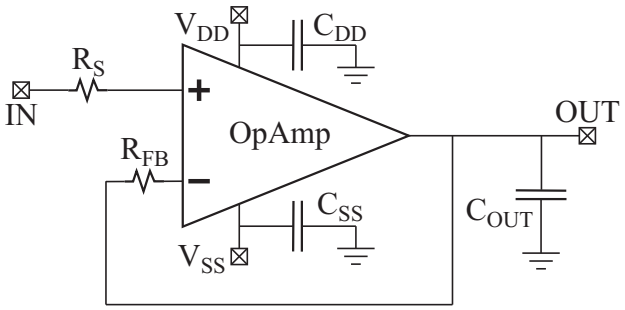


Figure 3.3: Schematic of the Devices under test (OpAmp connected as voltage follower).

Measurements of the input impedance

The input impedance of the DUT (Z_{DUT}) is evaluated through the reflection coefficient S_{11} measurement by:

$$Z_{DUT} = 50\,\Omega \frac{1 + S_{11}}{1 - S_{11}} \tag{3.15}$$

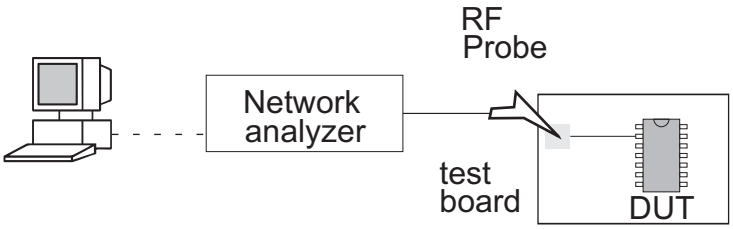


Figure 3.4: Test set-up for the measurement of the DUTs input impedance.

The test set-up is depicted in figure 3.4. The PC controlled (through Matlab code and the GPIB connection) the network analyzer (Agilent 8753ES) providing the frequency list and the power. Measurement results were sent back to the PC and stored for the post-processing (appendix B.1). The network analyzer was connected to the RF probe (Cascade Microtech P-04-N3S-SG-1270 |Z| probe) which directly contacted the PCB pad connected to the non-inverting input of the OpAmp under test. First the instrument was calibrated (one-port calibration with a calibration kit) and next the test fixture (the probe itself) was de-embedded to move the reference plane from the SMA tip to the PCB input pad. The de-embedding procedure was based on the measurement of the probe reflection coefficient and the mathematical removal of the test fixture characteristic from the overall measurement. The probe in short (tips connected together) and open condition (probe left in air) presents the reflection coefficients depicted in figure 3.5. As can be seen there is basically a

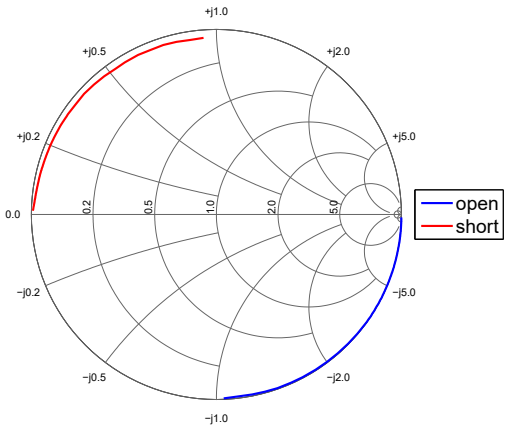
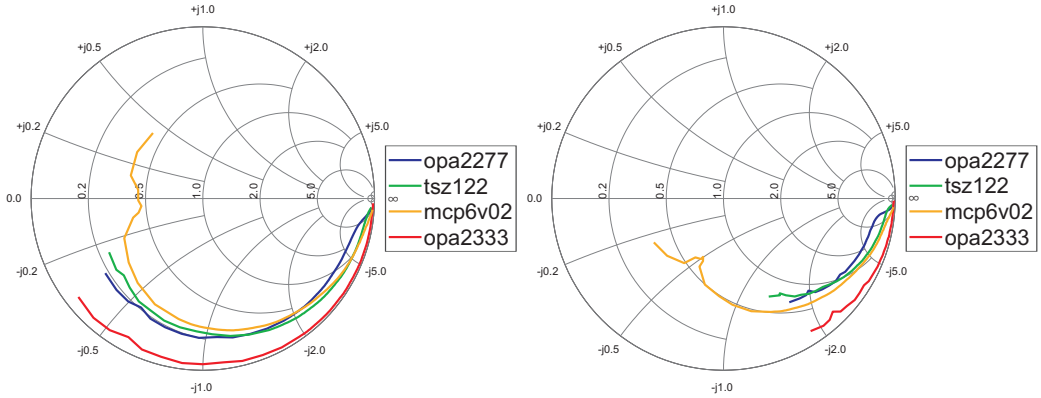


Figure 3.5: $|Z|$Probe reflection coefficient.

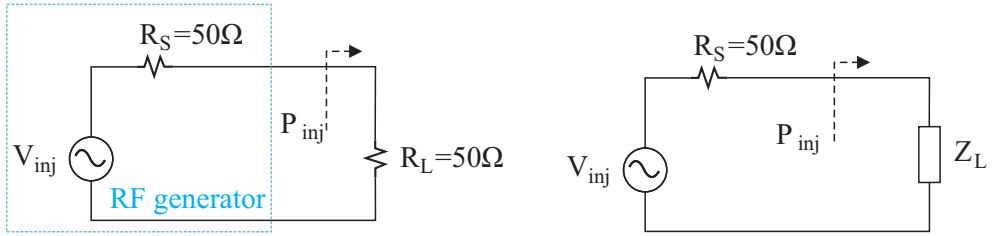
phase rotation for both the reflection coefficients and a bit of attenuation in the short condition. Such phase rotation can be de-embedded by introducing a delay of 118 ps in the network analyzer's port extension. In figure 3.6(a) and 3.6(b) there are the reflection coefficients of the DUTs before and after the de-embedding respectively.



(a) (b)

Figure 3.6: DUTs reflection coefficients before and after de-embedding.

OpAmps input voltage



(a) (b)

Figure 3.7: Circuits for the peak amplitude calculation. Matched load (a) and arbitrary load (b).

Disturbances are injected by a RF generator directly in the OpAmps input at a constant power of $P_{\text{inj}} = -15\,\text{dBm}$, $-10\,\text{dBm}$, $0\,\text{dBm}$, $5\,\text{dBm}$ and $10\,\text{dBm}$ (corresponding to $31.6\,\mu\text{W}$, $100\,\mu\text{W}$, $1\,\text{mW}$, $3.16\,\text{mW}$ and $10\,\text{mW}$). The RF generator can be considered as a voltage generator with a $50\,\Omega$ resistor in series as depicted in the blue box of Fig.3.7(a). The injected power level refers to the power of a matched load ($R_L = 50\,\Omega$):

$$P_{\text{inj}} = \frac{V_{RMS}^2}{R_L} = \left(\frac{V_{inj}}{2\sqrt{2}}\right)^2 \frac{1}{R_L} = \frac{V_{inj}^2}{8\ 50\,\Omega} \tag{3.16}$$

where V_{RMS} is the Root Mean Square voltage across the load resistor. The voltage provided by the ideal voltage generator V_{inj} is then

$$V_{inj} = \sqrt{8\ P_{\text{inj}}\ 50\,\Omega}. \tag{3.17}$$

The matched load resistor is then replaced by a generic load impedance Z_L and the RF peak voltage (V_p) is evaluated by the voltage divider:

$$V_p = \frac{Z_L}{Z_L + 50\,\Omega} V_{inj}. \tag{3.18}$$

The impedance ratio can be rewritten in term of reflection coefficient S_{11}, indeed:

$$S_{11} = \frac{Z_L - 50\,\Omega}{Z_L + 50\,\Omega} \tag{3.19}$$

and

$$1 + S_{11} = \frac{Z_L - 50\,\Omega + Z_L + 50\,\Omega}{Z_L + 50\,\Omega} = \frac{2\ Z_L}{Z_L + 50\,\Omega} \tag{3.20}$$

Substituting Eqn.(3.17) and (3.20) into (3.18) the RF peak voltage equation become:

$$V_p = \frac{1 + S_{11}}{2} \sqrt{8\ P_{\text{inj}}\ 50\,\Omega} = (1 + S_{11}) \sqrt{2\ P_{\text{inj}}\ 50\,\Omega} \tag{3.21}$$

Basically, the injected interference with power of $-15\,\text{dBm}$ translates into a maximum RF peak input voltage of 110 mV. Increasing the power, the input voltage increases as well, having 200 mV at $-10\,\text{dBm}$, $\approx 630\,\text{mV}$ at 0 dBm, 1.1 V at 5 dBm and finally 2 V at the highest injected power of 10 dBm.

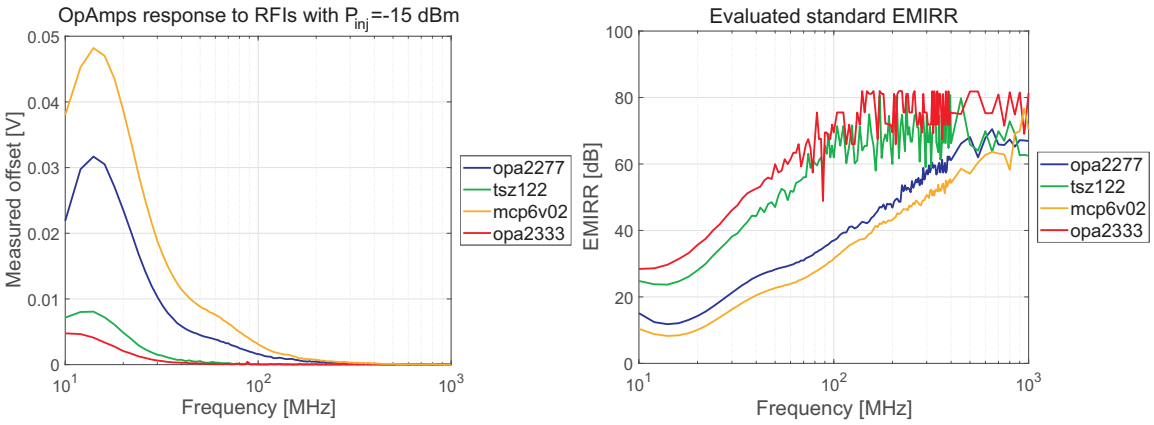
EMIRR evaluation

The EMIRR is evaluated with the measurement of the offset induced by the injection of RFIs with $P_{\text{inj}} = -15\,\text{dBm}$ and normalized to the standard test condition of 100 mV as defined in [36]. Fig.3.18(a) depicts the offset in absolute value, while in Fig.3.18(b) there is the evaluated EMIRR for all the OpAmps under test.

Some amplifiers, like the TSZ122 and OPA2333, exhibit an offset shift lower than µVs in the higher frequency range, thus it can be difficult to measure. This drawback, however, can be overcome by measuring the offset at higher power level and normalize after to the standard condition of 100 mV of input RF peak voltage. Nevertheless, these measurements are used to verify the offset prediction at higher injected power levels.

3.2.1 Comparison between EMIRR prediction and actual measured offset

Measurement results and the EMIRR predictions for each amplifier under test are briefly compared in the following.



(a) (b)

Figure 3.8: Measured RFIs induced offset (a) and standard EMIRR evaluated from measurement results (b).

The OPA2277 is a bipolar high-precision operational amplifier having ultra-low offset voltage (10 µV), high open-loop gain, CMRR and PSRR. Fig.3.9 presents the measured offset induced by the injection of CW interference in the OpAmp non-inverting input. The offset has a maximum between 10 MHz and 30 MHz and decrease for higher-frequency disturbance. At the highest injected power level the output clips to 1.5 V in the lower frequency range.

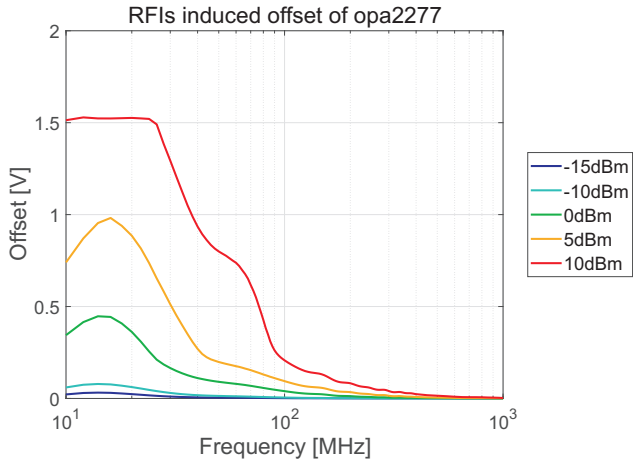


Figure 3.9: Measured RFIs induced offset of OPA2277 for all the injected RF power levels.

The offset evaluated with the EMIRR parameter for all the injected power levels is shown in Fig.3.10 in red, while the measured one is plotted in blue. As can be seen

such parameter provides an overestimation in the lower frequency range (10 MHz-100 MHz) and the deviation between the prediction and the measurement results increase as the power increases meaning that the square relationship between the square of the RF peak voltage and the offset is no more valid for such injected power levels. Nevertheless the EMIRR provide quite a good prediction for the −10 dBm injected disturbance, see Fig.3.10(a).

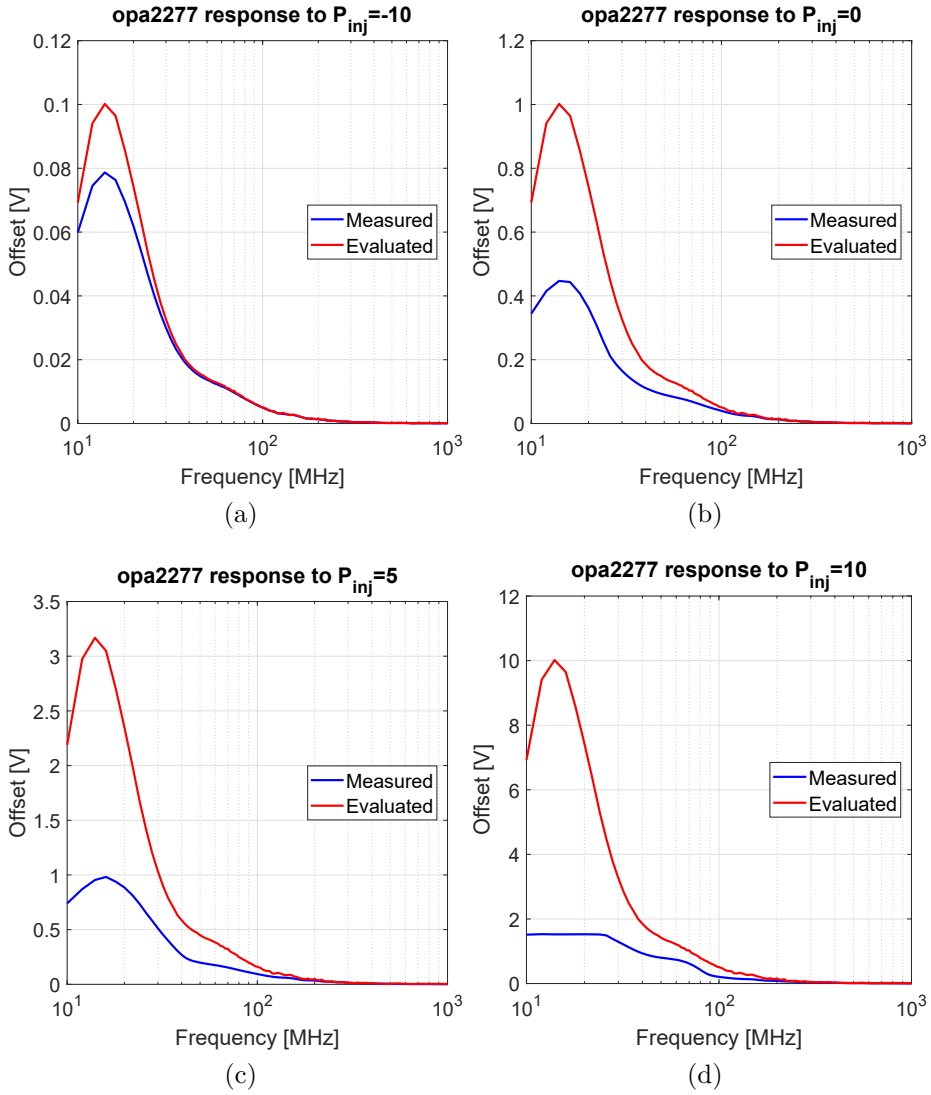


Figure 3.10: Measured and evaluated offset voltage of OPA2277 induced by RFIs injected at constant power of -10dBm (a), 0dBm (b), 5dBm (c) and 10dBm (d).

The OPA2333 is a CMOS low-offset (10 µV with auto-calibration), low quiescent current OpAmp optimized for low-voltage, single supply operation.

As can be seen from figure 3.11, the amplifier has really a good EMI immunity, the best among the devices under test. The RFI induced offset is negative with a maximum of about −0.9 V corresponding to the lower frequency disturbance injected (at the highest power level of 10 dBm). The EMI induced offset decreases as the frequency of the injected disturbance increases.

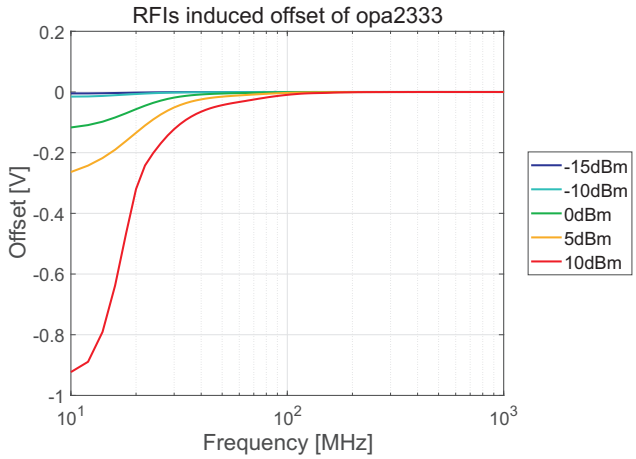


Figure 3.11: Measured RFIs induced offset of OPA2333 for all the injected RF power levels.

The comparison between the EMIRR prediction and the measurements is depicted in Fig.3.12. In this case the prediction overestimates the actual offset in the lower frequency range (from 10 MHz to 30 MHz) but can still be used as a worst case.

The difference between the evaluated offset and the measured one, which can better be seen in the log-log plot of Fig.3.13, highlights the drawback of the standard measurement. This OpAmp presents, indeed, a really low RFI induced offset at high frequency and it can be difficult to measure. It translates in wrong prediction in the higher frequency range (from 100 MHz to 1 GHz).

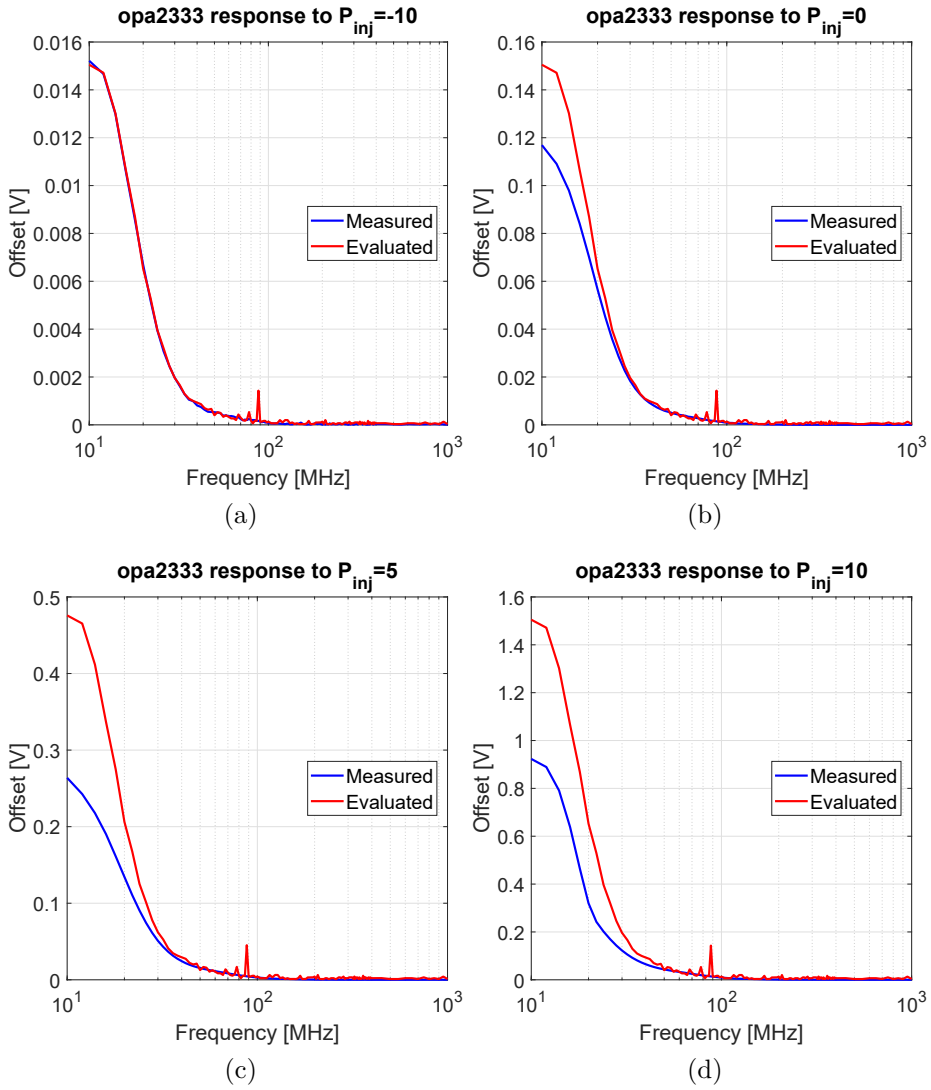


Figure 3.12: Measured and evaluated offset voltage of OPA2333 induced by RFIs injected at constant power of -10dBm (a), 0dBm (b), 5dBm (c) and 10dBm (d).

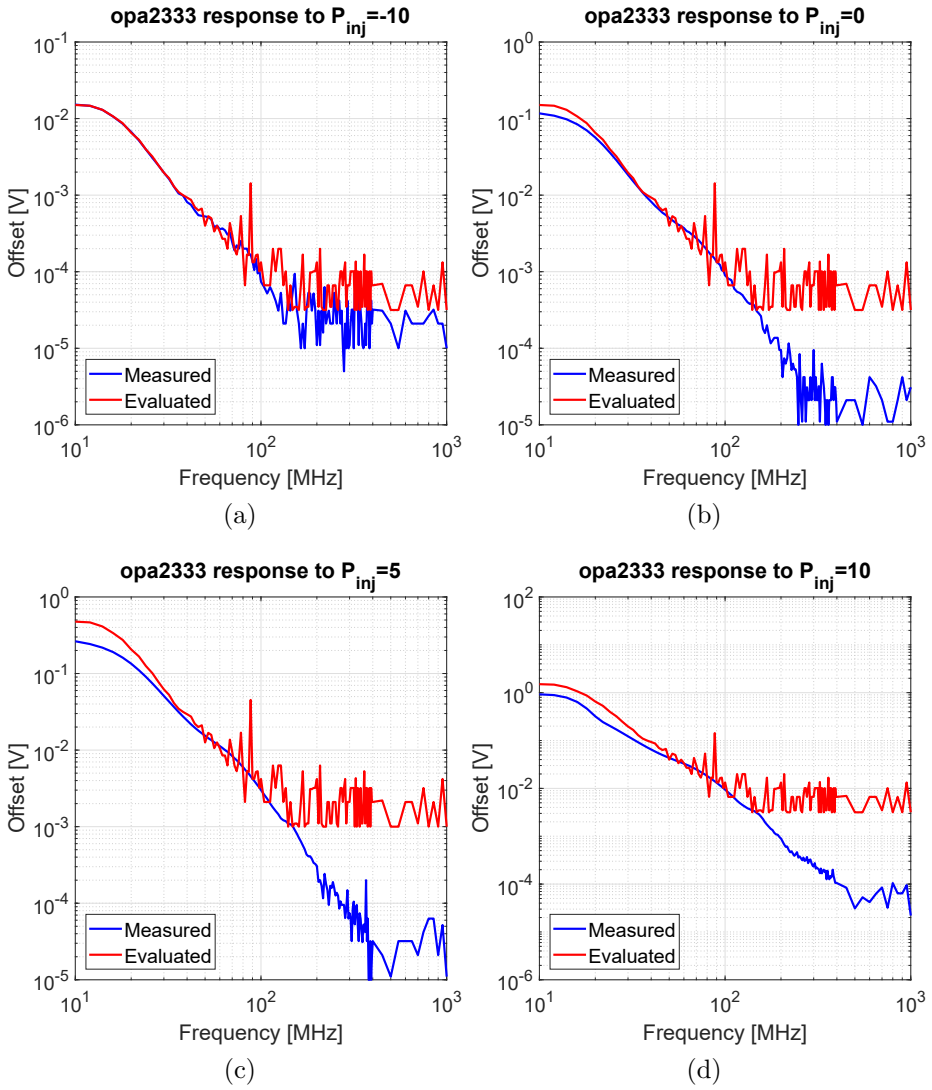


Figure 3.13: Measured and evaluated offset voltage of OPA2333 induced by RFIs injected at constant power of -10dBm (a), 0dBm (b), 5dBm (c) and 10dBm (d) in double logarithmic scale.

The TSZ122 is a very high accuracy (DC offset of 5 µV) micro-power operational amplifier using the chopper stabilized technique. Its datasheets reports also the EMIRR of the amplifier and it is claimed that the OpAmp is designed to minimize its susceptibility to EMI. It is true as long as the injected power does not exceeds 5 dBm as can be noticed in figure 3.14. For disturbance with power $\leq$5 dBm the offset is well bounded between 0 V and −0.4 V (being always negative) but for the interference with power of 10 dBm the output is practically always clipped to the positive power supply voltage of 2.5 V.

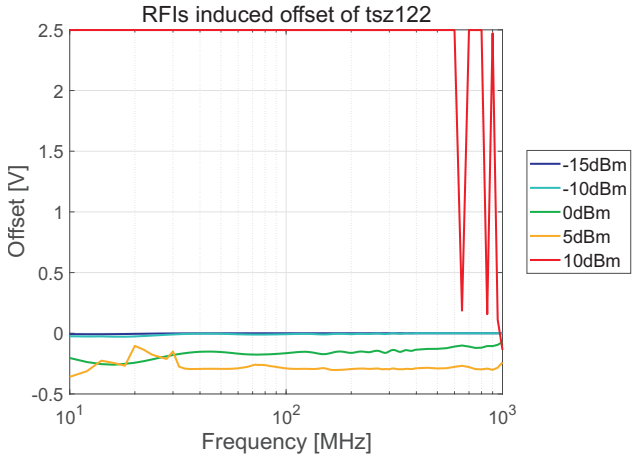


Figure 3.14: Measured RFIs induced offset of TSZ122 for all the injected RF power levels.

The comparison between the evaluation trough the EMIRR and the measurement results is depicted in Fig.3.15. In this case, the EMIRR practically fails all the prediction. This parameter guesses only the offset maximum between 10 MHz and 20 MHz except for the 5 dBm power level, see Fig.3.15(c).

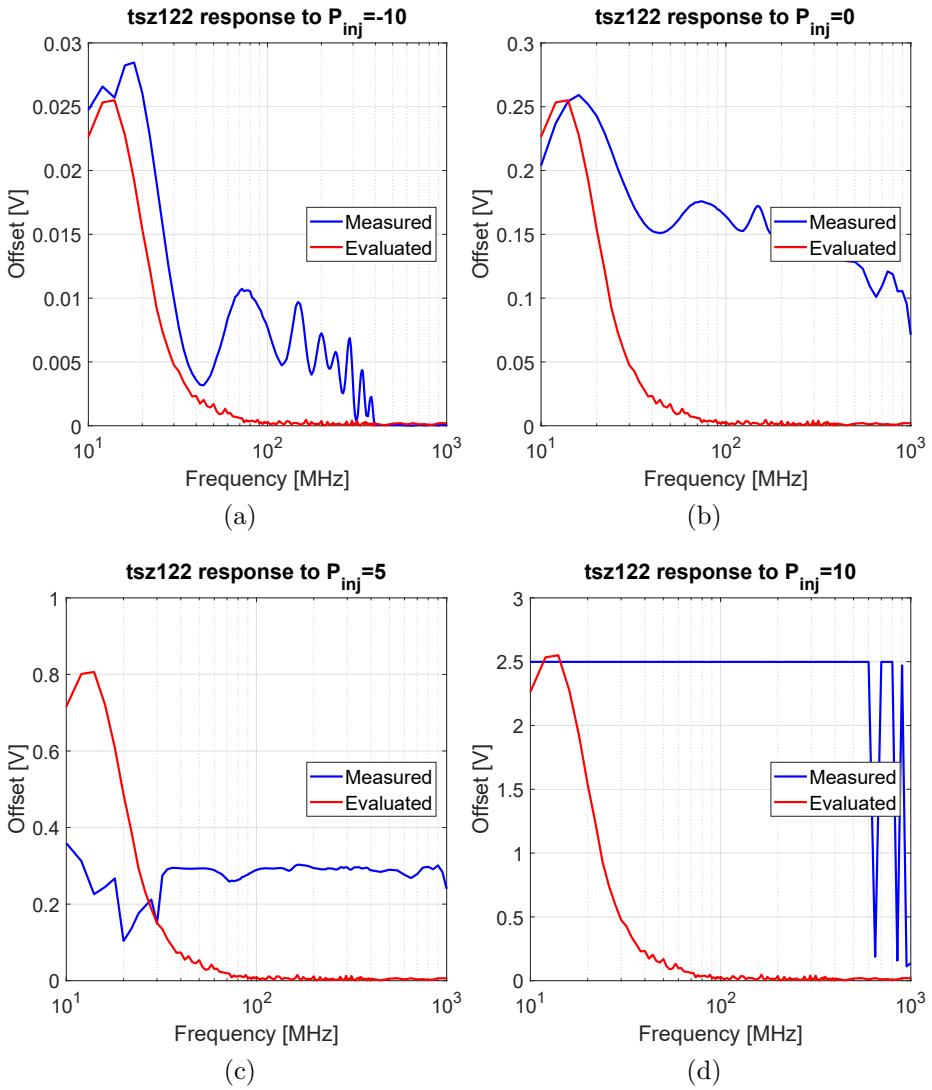


Figure 3.15: Measured and evaluated offset voltage of TSZ122 induced by RFIs injected at constant power of -10dBm (a), 0dBm (b), 5dBm (c) and 10dBm (d).

The MCP6V02 is designed for low-cost, low-power and high precision applications (low DC offset of about ±2 µV obtained by the auto-zero technique). The offset induced by the injection of RF disturbance in the input pin is negative for power levels ranging from −15 dBm to 5 dBm. The interference with the highest injected power (10 dBm) causes a positive offset shift for frequency lower than 27 MHz. The EMIRR, by definition, shall be calculated with the absolute value of the offset shift to avoid a negative argument of the logarithmic function, thus the sign and any change of sign of the actual offset is lost. This is another drawback of its definition.

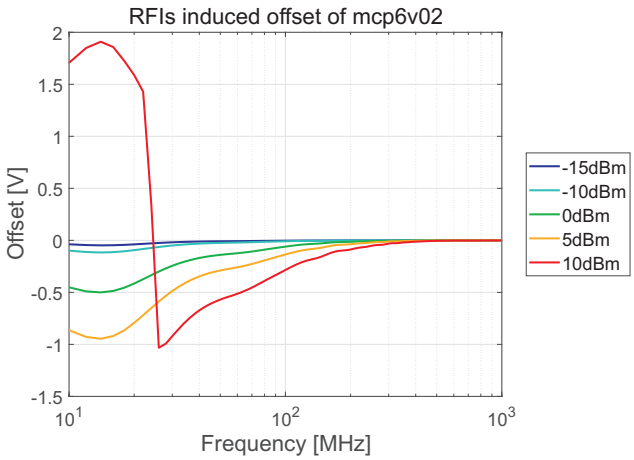


Figure 3.16: Measured RFIs induced offset of MCP6V02 for all the injected RF power levels.

The EMIRR predictions of figure 3.17 can be considered as the worst case only for the lower power injected disturbance −10 dBm but it is not acceptable for all other power levels: the overestimation is three times higher than the actual offset in the best case.

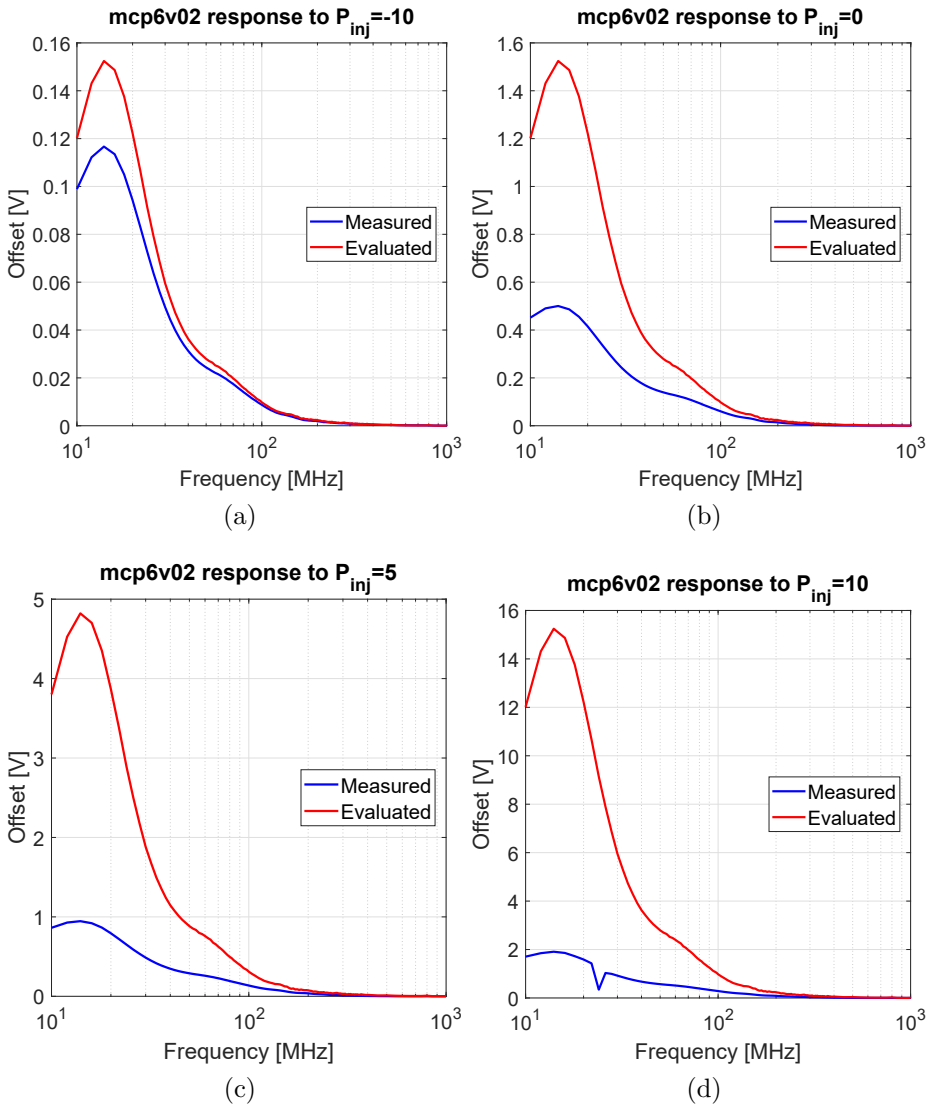


Figure 3.17: Measured and evaluated offset voltage induced by RFIs injected at constant power of -10dBm (a), 0dBm (b), 5dBm (c) and 10dBm (d).

3.3 Discussion

Two drawbacks were pointed out in this chapter. The first is strictly related to the EMIRR definition: the offset shift has to be taken in absolute value in order not to have a negative argument in the logarithm, thus this parameter hides any information about the sign of the offset. The second is related to the standard measurement condition of 100 mV of RF peak amplitude at the pin under test.

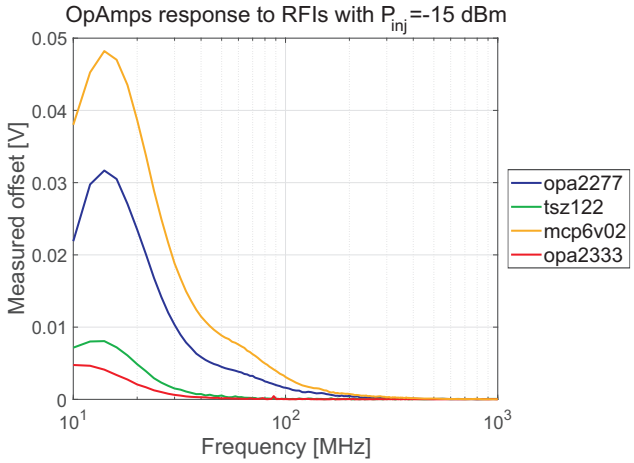
For EMI hardened OpAmps, the offset shift induced by the RFIs injection can be difficult to measure and it translates in wrong predictions; one example is provided by the OPA2333, Fig.3.13.

Nevertheless, the main limitation of the EMIRR parameter is the assumption of the quadratic relationship between the RFIs induced offset in OpAmps and the peak amplitude of the injected disturbance signal. In 3.1.1 it has been shown that such relationship is true if the differential pair (the most commonly used block as input stage of OpAmps) is the main upset contributor. Furthermore, its validity is limited to the weak non-linearity assumption: the voltage amplitude of the disturbance appearing between the gate and the source of the input MOSFETs (or between the base and the emitter for BJTs) should be lower than the overdrive voltage (or lower than the thermal voltage). Higher amplitudes can drive input transistors out of their designed operating region and eventually switch them on and off periodically.

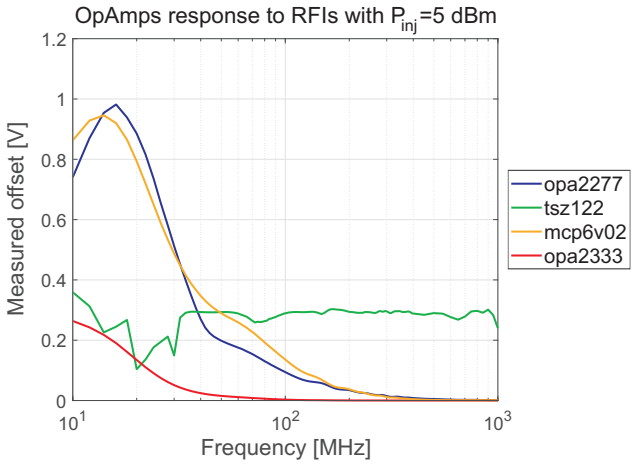
The analysis and measurement results proved that the EMIRR can be considered as a small-signal parameter. It is useful as long as the power of injected disturbance is low; for almost all the DUTs the predictions and the actual induced offset are in good agreement for an injected power level of $-10\,\mathrm{dBm}$ (corresponding to a RF peak voltage at the input of $\approx 200\,\mathrm{mV}$).

For higher power levels, the comparisons show that the EMIRR parameter fails to predict the voltage offset, especially in the low frequency range; for most the OpAmps it provides an overestimation. Another phenomenon that cannot be predicted is the output clipping, as shown by the response of the OPA2277 which output is constantly at $\approx$1.5 V for interference frequency lower than 23 MHz and the output of the TSZ122 that is clipped at the positive supply voltage of 2.5 V for almost all the disturbance frequencies.

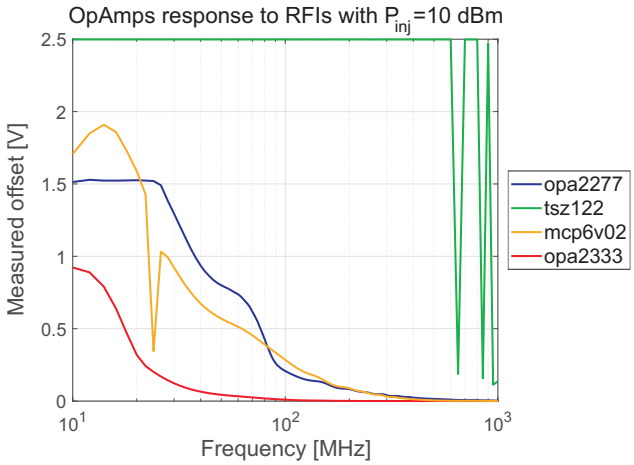
A better way to characterize and compare different OpAmps in terms of EMI immunity is to measure the actual offset at different RFIs power injections, like in Fig.3.18. In this plot there is the actual measured offset (in absolute value) for all the OpAmps under test and for three different power levels. Figure 3.18(a) refers to the injection of RFIs with power of $-15\,\mathrm{dBm}$ while in figure 3.18(b) and (c) there is the offset induced by disturbance with power of $5\,\mathrm{dBm}$ and $10\,\mathrm{dBm}$. These figures show that the response of OpAmps to high-power EMI is unpredictable from their response to low-power injected interference.



(a)



(b)



(c)

Figure 3.18: Measured offset induced by RFIs injected at constant power of -15dBm (a), 5dBm (b) and 10dBm (c).

Chapter 4

Susceptibility of OpAmps to Multi-Tone Interference

The robustness of ICs to EMI is usually evaluated by means of analysis and measurements, e.g. the DPI method. This is based on the continuous wave interference that is an unmodulated sinusoidal signal. For each frequency, the injected power is increased until the monitored output is brought to a specified failure, i.e. the susceptibility criterion, or until the maximum power is reached. In this way the susceptibility profile of the DUT is evaluated and reported usually in graphs like the one of Fig.2.16. The IEC 62132-4 defines as well a reference modulated signal to be injected: the interference can be amplitude modulated with a 1 kHz sine wave. In this case, the peak power shall be the same as the one of the CW counterpart. The use of the AM disturbance is not mandatory and the CW approach is the preferred one and it has never being questioned. The main drawback is that real-life EMI, e.g. generated by wireless communications, power switching circuits, or radio and TV broadcasting, cannot be reduced to simple sinusoidal signals.

For example, an IC placed nearby a short-range wireless transmitter can be subjected to interference caused by Bluetooth communication. This technology operates in the 2.4 GHz ISM band and the maximum transmitted power shall be bounded to 100 mW. Moreover, the communication band is subdivided in 79 channels with 1 MHz bandwidth and binary data (with 1 MBit/s of symbol rate) are transmitted using the GFSK modulation, thus they are represented by a small frequency deviation.

The susceptibility of the IC could be tested, following the CW approach, by injecting only the interference with frequency equal to the channel center frequency. However, this method does not ensure to cover all the possible failures induced by actual interference. For example, BLE uses a time division duplex scheme for full duplex transmission: the master and the slave transmit alternately. The basic piconet physical channel is divided into time slots of 625 µs and packets may extend

up to five consecutive time slots. If the slave responds with the acknowledgment only (thus occupying a single time slot) and the master transmits all the different packet formats, the channel occupation become the one depicted in Fig.4.1. The resulting interference is most likely a high-frequency signal multiplied by a square wave with variable frequency and duty cycle. It can be seen also as an OOK modulation where the data rate is the inverse of the basic time slot and the binary number 1 are represented by the transmitter channel occupation.

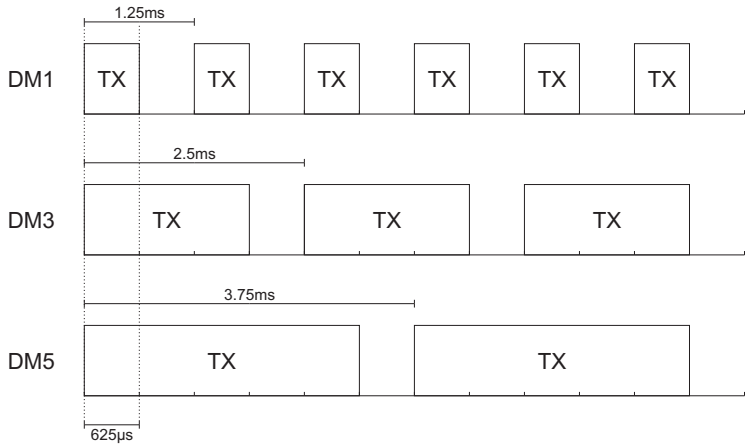


Figure 4.1: Example of channel occupation (Standard Bluetooth communication).

The same reasoning applies to all the RF communications employing the Time Division Multiple Access (TDMA), e.g. the GSM-900 in uplink. In such case, the basic TDMA frame has a duration of 4.62 ms and it is subdivided in 8 time slots of 576.9 µs. In the worst case, the data are transmitted with a maximum power of 2 W (GMSK modulated, carrier within 890 MHz-915 MHz). Again, the disturbance generated by the GSM communication is similar to a high-frequency burst with low-frequency repetition rate. The effect of such kind of interference coupled onto the input of a feedback amplifier is highlighted in Fig.4.2. In this simulation, the applied interference is an out of band CW signal periodically switched on and off (same timing of the Bluetooth DM1 packets, Fig.4.1). The output waveform is essentially a square wave with a high frequency component superimposed on the positive semi-period. This practical example points out the need of identifying the possible failures affecting ICs when exposed to real EM environment.

The effects of multi-tone interference in feedback OpAmps were discussed to this purpose. Depending on the frequency spacing between interfering tones, two effect arose: the output DC offset and the beat component in case of intermodulation distortion. The latter is also investigated through measurements by means of an affordable test setup as shown in Section 4.2.

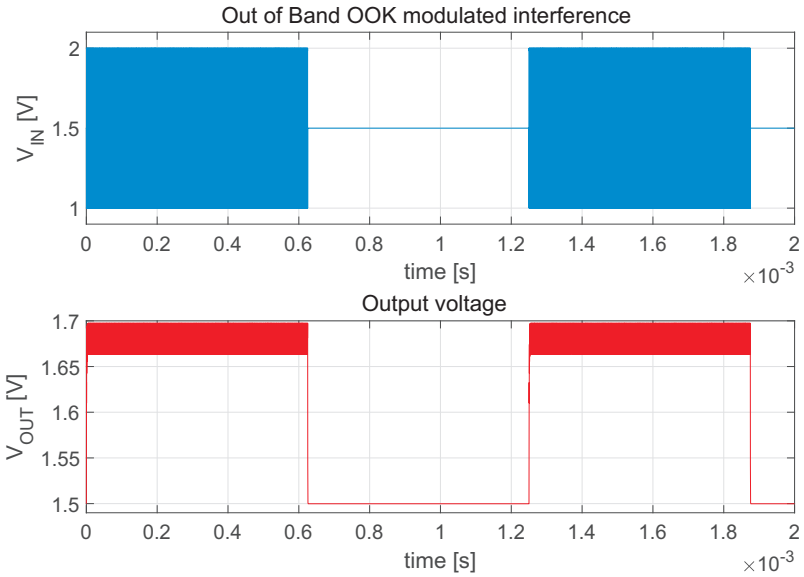


Figure 4.2: Simulated upset induced by OOK modulated interference.

4.1 Multi-tone analysis

In the following analysis the effect of a multi-tone injection in the OpAmp connected as voltage follower is investigated. The model of (2.14) is based on the weak non-linearity assumption and the small signal analysis, thus the superposition principle applies too: the circuit is practically linearized around its operating point. The generic multi-tone input waveform can be described as a sum of sinusoidal signal as:

$$V_+(t) = \sum a_n cos\Big(\omega_n t\Big) \tag{4.1}$$

where a_n and ω_n are arbitrary amplitudes and angular frequencies such that the maximum of $V_+(t)$ does not lead the transistors out of the saturation. The differential mode input voltage is obtained by substituting the Fourier transform of Eqn.(4.1) into (2.20) and performing the inverse Fourier transform as in Eqn.(2.22).

$$v_d = \sum a_n \ |K_d(j\omega_n)| \ cos\Big(\omega_n t + \angle K_d(j\omega_n)\Big) \tag{4.2}$$

Similarly the Fourier transform of Eqn.(4.1) is used in Eqn(2.21) and the result substituted into the equation (2.17). The inverse Fourier transform leads to the following expression for the effective bias current fluctuation:

$$i = \sum \ |I(j\omega_n)| \ cos\Big(\omega_n t + \angle I(j\omega_n)\Big) \tag{4.3}$$

The differential drain current is then evaluated by substituting (4.2) and (4.3) into Eqn.(2.14).

$$i_d = g_m \sum a_n \; |K_d(j\omega_n)| \; cos\Big(\omega_n t + \angle K_d(j\omega_n)\Big) + \\ + g_p \left(\sum a_n \; |K_d(j\omega_n)| \; cos\Big(\omega_n t + \angle K_d(j\omega_n)\Big)\right) \times \left(\sum |I(j\omega_n)| \; cos\Big(\omega_n t + \angle I(j\omega_n)\Big)\right) \tag{4.4}$$

the first term is a sum of sinusoid, it is periodic and with zero mean value. For this reason it does not provide any offset contribution. The second term contains n^2 products of *cos* functions, where only the products of sinusoid with the same frequency (according to 2.25) contribute to the RFI induced offset. It can be expressed as:

$$\Delta V_{off\ n} = \frac{g_p \sum a_n \; |K_{dn}| \; |I_n| \; cos\Big(\angle I_n - \angle K_{dn}\Big)}{2 g_m} \tag{4.5}$$

were K_{dn} and I_n are used to express $K_d(j\omega_n)$ and $I(j\omega_n)$ in a more compact form. Moreover, the offset induced by the sum of sinusoidal signals is equal to the sum of the offset that any signal will generates (superposition of effects), that is:

$$\Delta V_{off\ n} = \sum_n \Delta V_{off}(n) \tag{4.6}$$

The remaining products of Eqn.(4.4) can be written as the sum of two *cos* functions with frequency equal to the sum and the difference of ω_1 and ω_2 as follows:

$$cos(\omega_1 t + \phi_1)\; cos(\omega_2 t + \phi_2) = \frac{1}{2}\Big[cos(\omega_1 - \omega_2 + \phi_1 - \phi_2) + cos(\omega_1 + \omega_2 + \phi_1 + \phi 2)\Big]. \tag{4.7}$$

All of these products have zero mean value but in the case of $\omega_1 - \omega_2 < GBW$ the first term in the right hand side appears at the output as the beat component caused by intermodulation. It can be further simplified by

$$\begin{aligned} cos(\omega_1 - \omega_2 + \phi_1 - \phi_2) &= cos(\omega_1 - \omega_2) cos(\phi_1 - \phi_2) - sin(\omega_1 - \omega_2) sin(\phi_1 - \phi_2) \\ &\approx cos(\omega_1 - \omega_2) cos(\phi_1 - \phi_2) \end{aligned} \tag{4.8}$$

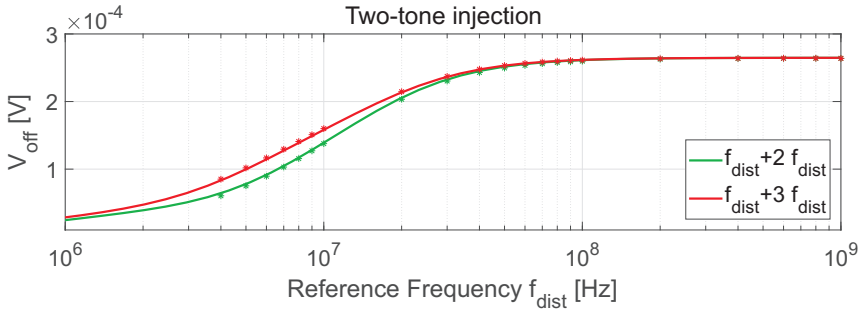
if $\phi_1 \approx \phi_2$ which implies $sin(\phi_1 - \phi_2) \approx 0$.

Summarizing, if two tones with $\omega_1, \omega_2 \gg GBW$ are spaced by $\Delta\omega \ll GBW$, the output will have components within the amplifier bandwidth. The peak amplitude V_{pim} of the in-band beat component of the demodulated interference can be expressed as:

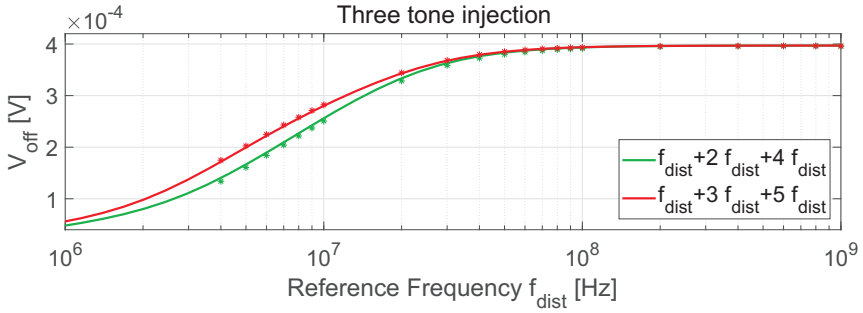
$$V_{pim} \approx \frac{a_1 |K_{d1}| \; |I_2| cos\Big(\angle I_2 - \angle K_{d1}\Big)}{2} + \tag{4.9}$$

$$+ \frac{a_2 |K_{d2}| \; |I_1| cos\Big(\angle I_1 - \angle K_{d2}\Big)}{2} \tag{4.10}$$

4.1.1 Offset induced by multi-tone injection



(a)



(b)

Figure 4.3: Simulated (stars) and modeled (line) offset induced by the injection of the multi-tone disturbance. Two-tones (a) and three-tones (b) injection. Each tone has an amplitude of 10 mV.

In Fig.4.3 there are the simulation results (stars) and the modeled offset (straight lines) of the OpAmp subjected to the multi-tone injection at the non-inverting input. The amplitude of each disturbance is 10 mV ensuring the weak non-linearity, indeed in the worst case the sum of the peaks of the interfering signal is bounded by 30 mV (which is lower than the input transistor overdrive voltage). The lower-frequency of the injected signal is taken as reference and the second and third tones were derived from it. Both the simulated offset and the amplitude of the beat component were plotted over the reference frequency abscissa, i.e. $V_{off}(10\,\text{MHz} + 20\,\text{MHz}) = V_{off}(f_{dist} + 2\ f_{dist})$ is plotted above the 10 MHz abscissa.

In Fig.4.3(a), there is the plot of the offset induced by an interference made up of two sinusoids having frequency one double the other (green line). The red plot refers to the injection of a two-tone signal where the ratio between the two frequencies is set to three, that is $V_{dist}(t) = 10\,\text{mV}sin(\omega_{dist}t) + 10\,\text{mV}sin(3\ \omega_{dist}t)$. The plot of Fig.4.3(b) refers to the injection of three sinusoids with frequencies that are even integer multiple of the reference one ($\sum_{tones} f_{dist} + 2f_{dist} + 4f_{dist}$ in green) while in

red the three frequency are odd integers of f_{dist}, i.e. $\sum_{tones} f_{dist} + 3f_{dist} + 5f_{dist}$. As can be seen the model prediction is in good agreement with the simulation results over all the frequencies considered.

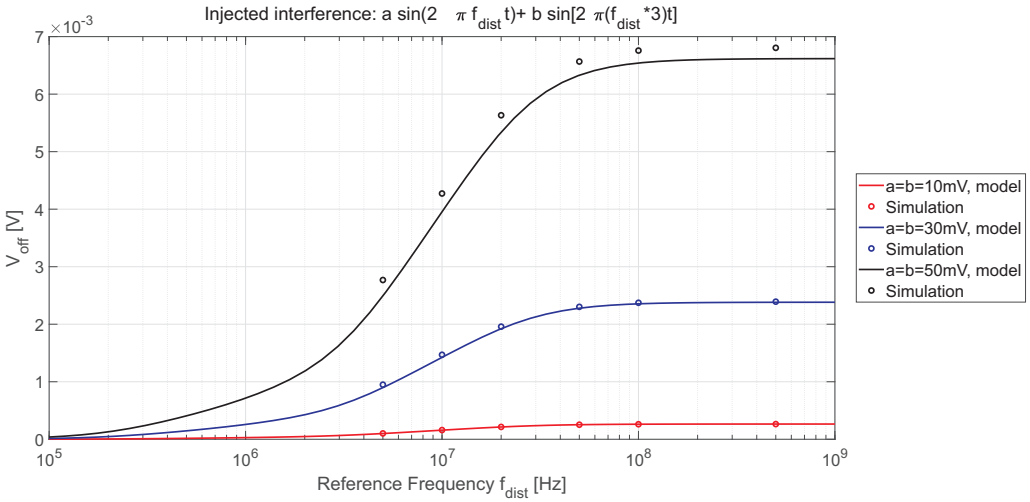
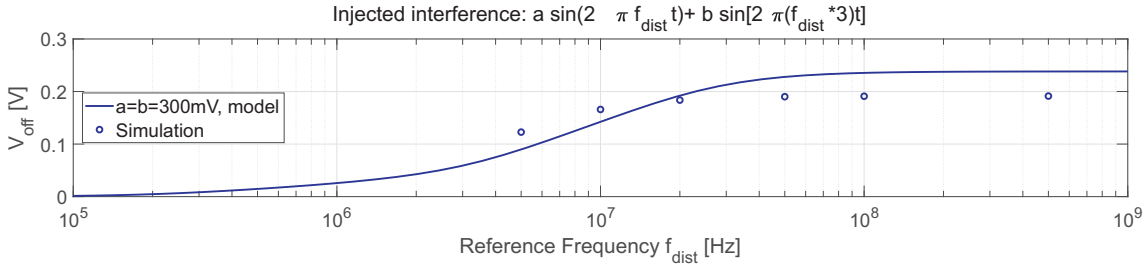
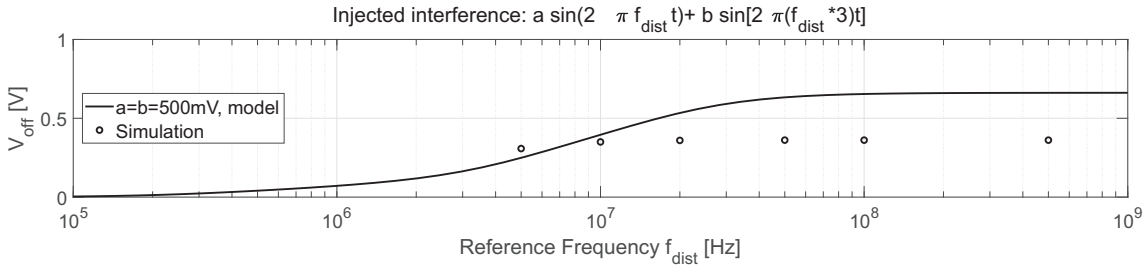


Figure 4.4: Simulated and modeled offset induced by the injection of a two-tone disturbance for the model validity analysis.



(a)



(b)

Figure 4.5: Simulated and modeled offset induced by the injection of a two-tone disturbance for the model validity analysis. (RF amplitudes $\gg V_{OD}$).

The validity of the model has been verified, as in section 2.2.1, by increasing the amplitude of the tones (it has been kept equal for both of them). In Fig.4.4 the amplitude of each tone is kept lower than the input transistor overdrive voltage ($V_{OD} \approx 55\,\text{mV}$). The model prediction deviates from simulation results only for the higher amplitudes, indeed the maximum of the disturbance waveform (for $a = b = 50\,\text{mV}$ it is $\approx 77\,\text{mV}$) is higher than V_{OD} and the device is periodically brought out of the saturation region.

The amplitude of each tones is then increased to 300 mV and 500 mV as depicted in Fig.4.5(a), and (b) respectively. The model does not provide any useful offset estimation: the maximum of the applied interference, indeed, is $\gg V_{OD}$. The behavior of the estimations with respect simulation results is in accordance with the discussion of section 2.2.1 and Fig.2.8.

4.1.2 Intermodulation distortion

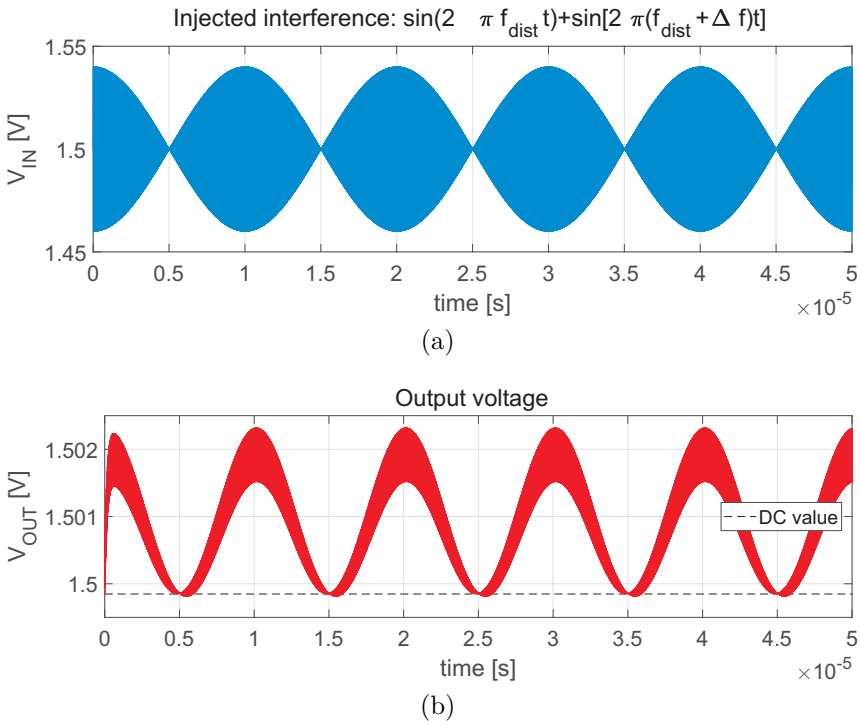
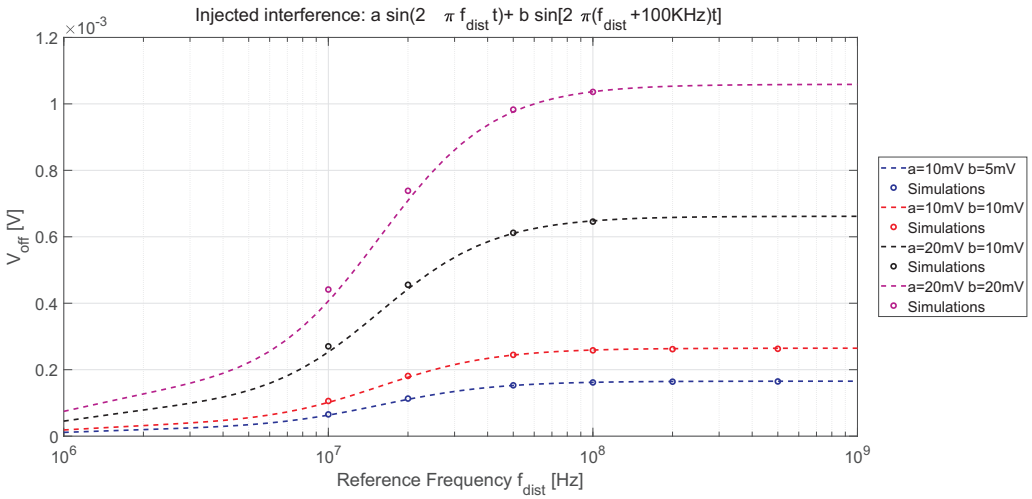


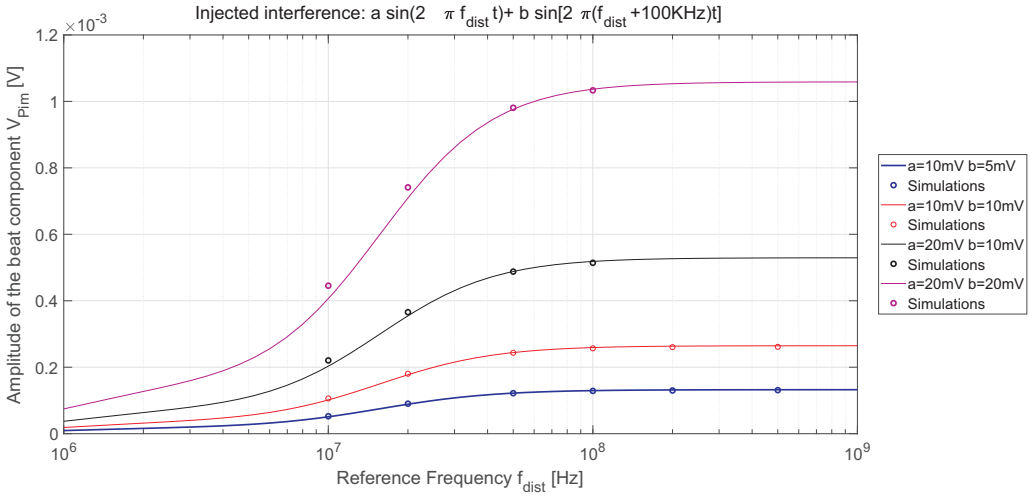
Figure 4.6: Transient simulation highlighting the intermodulation distortion effect.

The intermodulation distortion is simulated injecting an interference that is the sum of two sinusoids with frequency spacing within the amplifier's bandwidth ($\Delta f \ll 1\,\text{MHz}$). The output is affected by both an offset voltage and by a sinusoid

with frequency equal to Δf as shown in Fig.4.6. This plot shows the transient simulation of the OpAmp subjected to the injection of two tones (same amplitude of 20 mV) of f_{dist} =100 MHz and $f_{dist} + \Delta f$ =100 MHz+100 kHz, see Fig.4.6(a). The output voltage is plotted in the figure Fig.4.6(b) in red and its DC value (with no interference applied) is highlighted with the dashed black line.



(a)



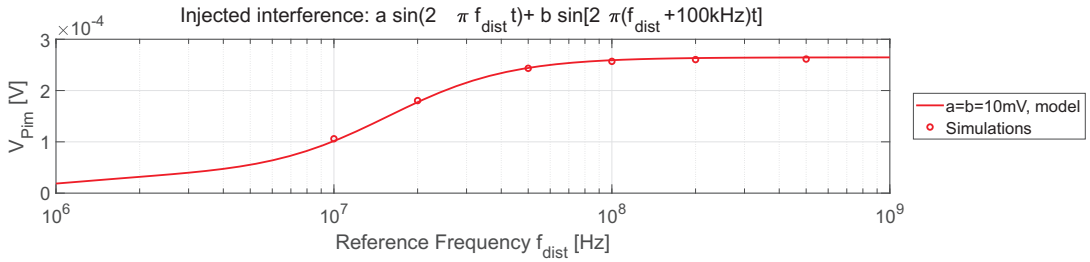
(b)

Figure 4.7: Comparison between model prediction and simulation results for the intermodulation analysis. Offset voltage (a) and beat component amplitude (b).

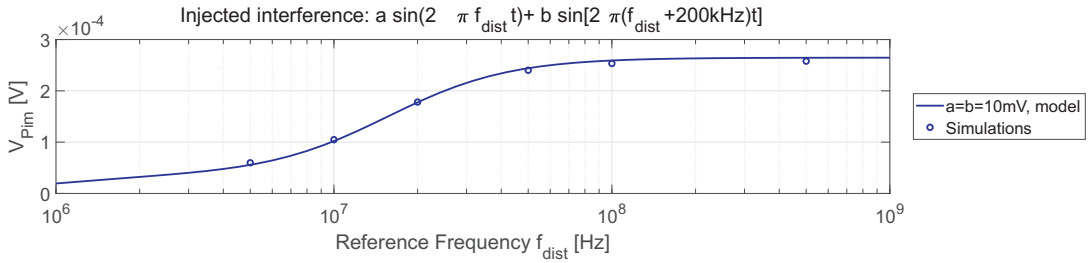
Given that the period of the output voltage will be set by $T_{im} = 1/\Delta f \gg 1/f_{dist}$, the offset should be then calculated averaging the output voltage clipped for at least one T_{im} after the steady state is reached. Therefore, the simulation

of the intermodulation distortion requires much more time to be carried out. The amplitude of the beat component is evaluated directly in Cadence by the calculation of the discrete Fourier transform of the clipped output waveform.

Fig.4.7(a) shows the comparison between the modeled offset voltage (dashed lines) and the simulation results (circles). In Fig.4.7(b) there are the plots of the amplitude of the beat component V_{Pim} evaluated trough the analytical model (continuous lines) and extracted from simulations (circles). The reference frequency f_{dist} is varied from 10 MHz to 500 MHz and the difference between the frequencies of the two tones is kept constant (100 kHz). The amplitude of the tones is changed from 5 mV to 20 mV as explained in the legends. As can be seen, if the amplitudes of the two tones are equal, the offset voltage is also a good indication of the amplitude of the low frequency beat component. In the case of tones with different amplitudes, the amplitude of the beat component caused by the intermodulation distortion is lower than the RFIs induced offset and it has to be calculated with Eqn.(4.9). The comparison between the model prediction and the simulations shows a good agreement.



(a)

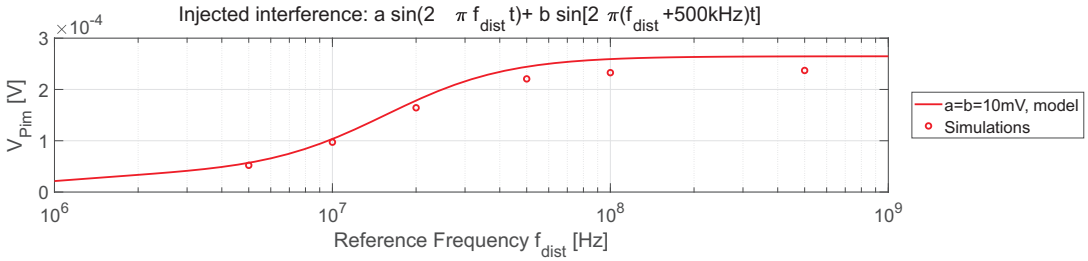


(b)

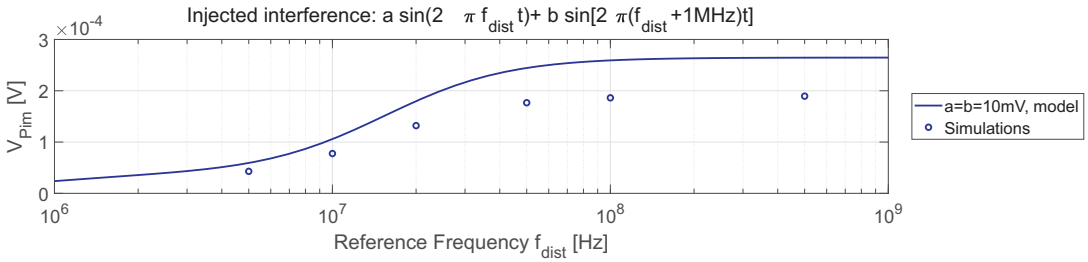
Figure 4.8: Comparison between model prediction and simulation results for the intermodulation analysis. Δf = 100KHz (a) and Δf =200KHz (b).

The validity of the model has been analyzed by increasing both the frequency spacing Δf and the tones amplitude. Fig.4.8 refers to simulations in which the amplitude has been kept to 10 mV for both tones and the frequency spacing is much lower than the amplifier's bandwidth. The analytical model provides good

estimations for the beat component amplitude. Δf is then increased to half the bandwidth (500 kHz) as reported in Fig.4.9(a) and to 1 MHz, see Fig.4.9(b). The model provides an overestimation of the beat component amplitudes evaluated from simulation results. It means that the model validity is limited to $\Delta f \ll GBW$.



(a)



(b)

Figure 4.9: Comparison between model prediction and simulation results for the intermodulation analysis. $\Delta f = 500\,\text{kHz}$ (a) and $\Delta f = 1\,\text{MHz}$ (b).

In the next set of simulations the amplitude of the interfering waveform is increased in order to drive the transistor out of the designed operating region (saturation). Fig.4.10 reports the model predictions and the simulation results for a two tone injected interference where $\Delta f = 1\,\text{MHz} = GBW$ and the amplitude of each tone is increased to 30 mV and 50 mV. The analytical model provides good results for the offset prediction, Fig.4.10(a) while the amplitude of the beat component is underestimated, see Fig.4.10(b). The tones amplitude is further increased to 100 mV and it leads the model out of its validity region. The prediction of the offset voltage of Fig.4.11(a) underestimates the simulated ones (as in section 2.2.1 and 4.1.1) while the amplitude of the beat component, see Fig.4.11(b), is underestimated.

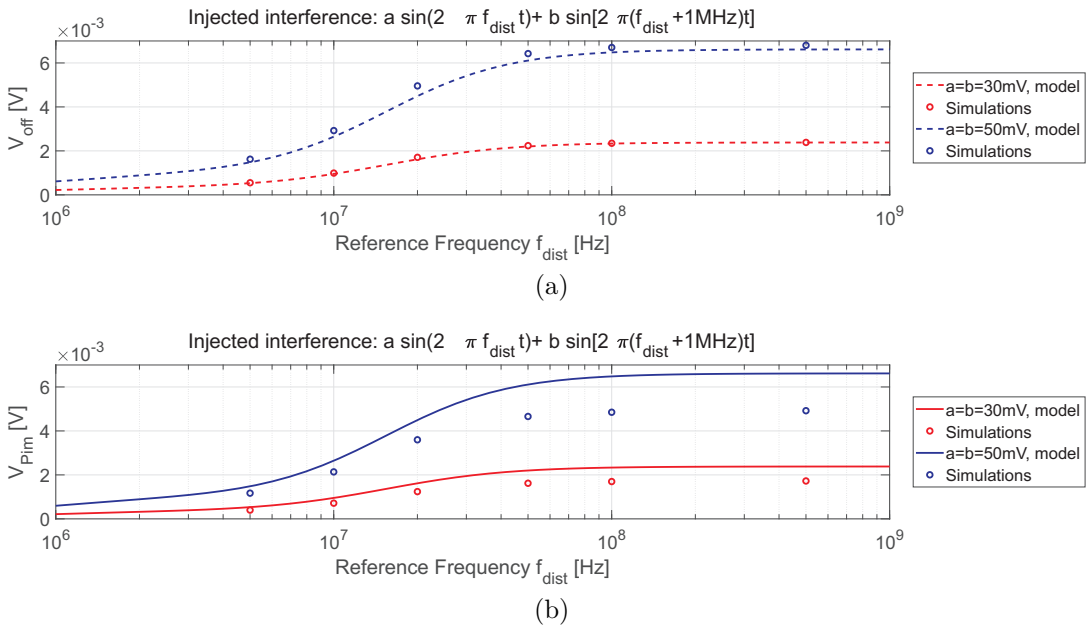


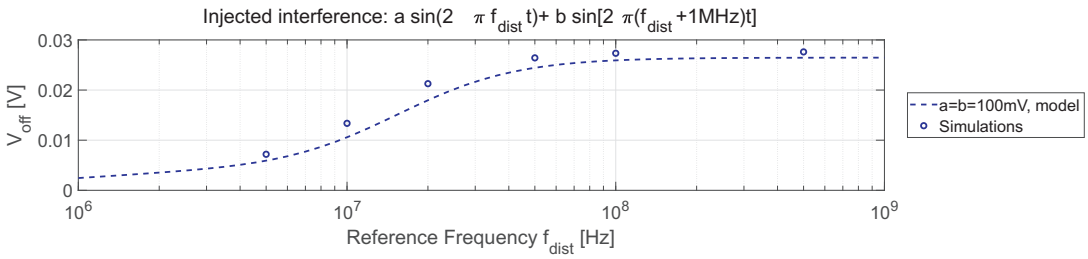
Figure 4.10: Comparison between model prediction and simulation results for the intermodulation analysis $\Delta f = 1\,\text{MHz}$. Offset voltage (a) and beat component amplitude (b).

4.1.3 Discussion

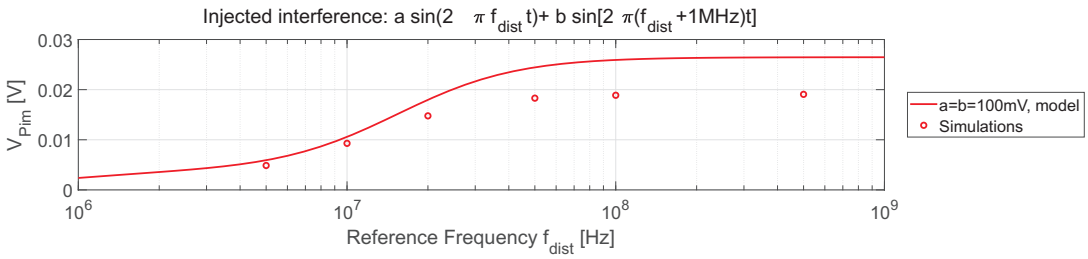
Actual EMI cannot be modeled only as CW signals and more accurate analysis should be performed on analog circuits. Two effects arising from the injection of a multi-tone interference in feedback OpAmps have been discussed. The analytical model provides good agreement with simulation results under the assumption of weak non-linearity (i.e. transistors working in the saturation region).

If the frequency spacing between tones is greater than the OpAmp gain per bandwidth product, the main effect is the generation of a DC offset at the output. It can be predicted as the sum of the contribution of each sinusoid. On the other hand, if the frequency spacing between two tones is $\Delta f \ll GBW$ the intermodulation distortion will cause the appearing of the beat component (signal with frequency equal to Δf).

The proposed analytical model has been validated by the comparison with the simulations of a practical OpAmp connected as voltage follower.



(a)



(b)

Figure 4.11: Comparison between model prediction and simulation results for the intermodulation analysis $\Delta f = 1\,\mathrm{MHz}$. Offset voltage (a) and beat component amplitude (b).

4.2 Susceptibility measurements with two-tone interference

A multi-tone interference superimposed onto the input of a feedback amplifier induces not only a DC offset shift in its output but also the beat of the RF tones. This latter effect cannot be evaluated with standardized immunity tests which are mainly carried out with CW interference. If the victim circuit has a bandpass response, e.g. audio amplifier for microphones or accelerometers, the DC offset induced by the CW testing will not affect the output, thus the DUT will seem to be immune to interference. Nevertheless, the reliability of these circuits is compromised by actual EMI, which are usually modulated or composed by several spectral components. The intermodulation products can fall within the bandwidth of circuits leading to failures. To this purpose an affordable test setup to cover the intermodulation effects is proposed; its block diagram is shown in Fig.4.12. The two-tone interference is made by the combination of the outputs of two independent RF sources through the combiner. Its output feeds a wideband RF amplifier whose output is monitored by the spectrum analyzer connected to the directional coupler. The high frequency two-tone interference is then summed (thanks to the bias tee) to the DUT bias, which is provided by the LF/DC generator. The output of the DUT (TS912 OpAmp) is

monitored by an oscilloscope.

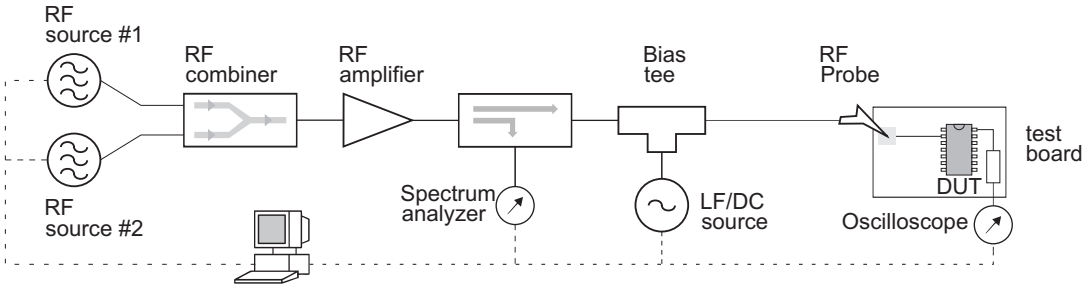


Figure 4.12: Test setup for the two-tone susceptibility measurements.

The comparison between a standard measurement, that is a CW injection, and the two-tone injection is reported in Fig.4.13 where the OpAmp output voltage is plotted vs. time. When the amplifier is subjected to the CW interference with frequency of 100 MHz and power −4 dBm, the output (violet plot) experiences a DC offset shift only. In the case of Two-Tone injection at 100 MHz and frequency deviation of 400 Hz the beat component appears in the output as shown in red, where the injected power of each tone is −9 dBm, and in black (P_{inj} =−4 dBm).

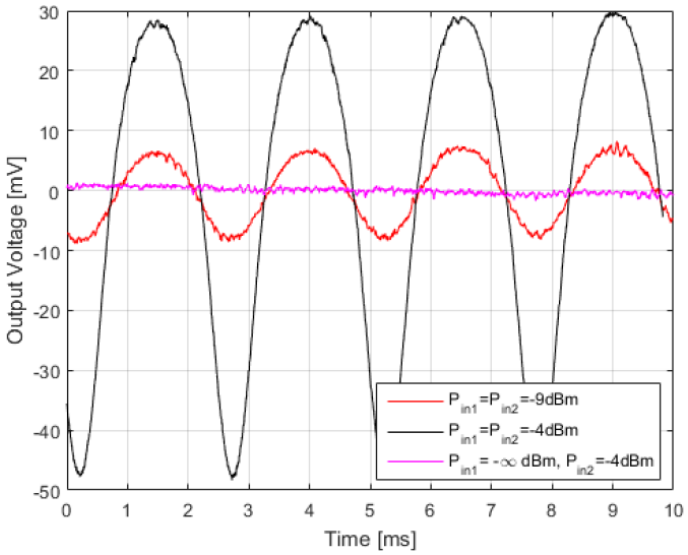


Figure 4.13: Measurement results comparing the effects induced by the CW and the two-tone injection.

The output voltage DC offset induced by a two-tone injection with frequency spacing of 400 Hz (within the bandwidth) and 10 MHz (out of bandwidth) is then compared with the injection of the single tone having equal injected power. Measurements were made by varying the injected power and fixing the frequency to

100 MHz, 450 MHz and 900 MHz as reported in Fig.4.14, 4.15 and 4.16 respectively. As can be seen, the offset induced by the two-tone interference is comparable to the one induced by the CW injection having injected power equal to the sum of the two.

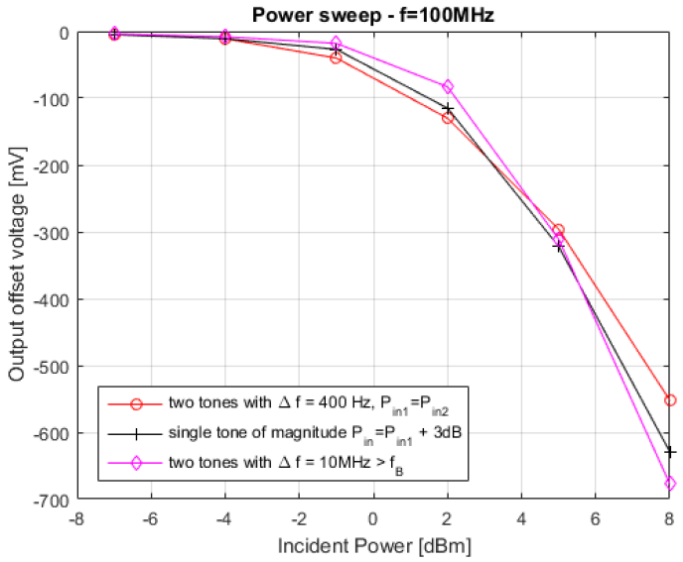


Figure 4.14: Measurements of the OpAmp output voltage offset induced by interference injection at 100 MHz.

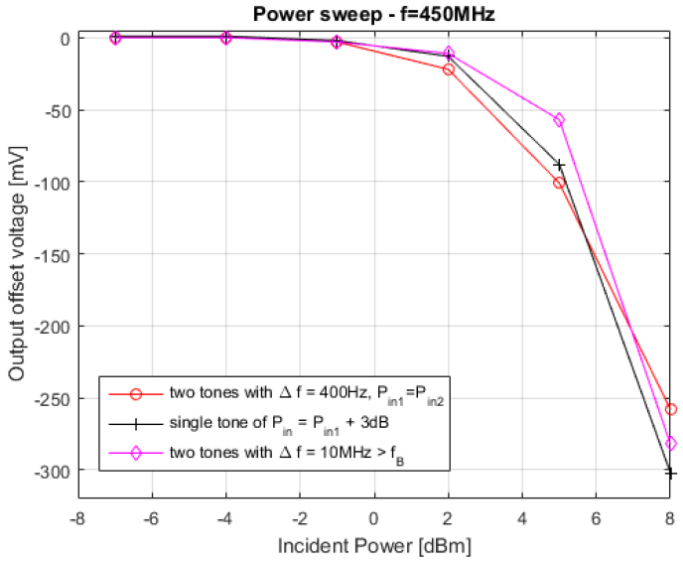


Figure 4.15: Measurements of the OpAmp output voltage offset induced by interference injection at 450 MHz.

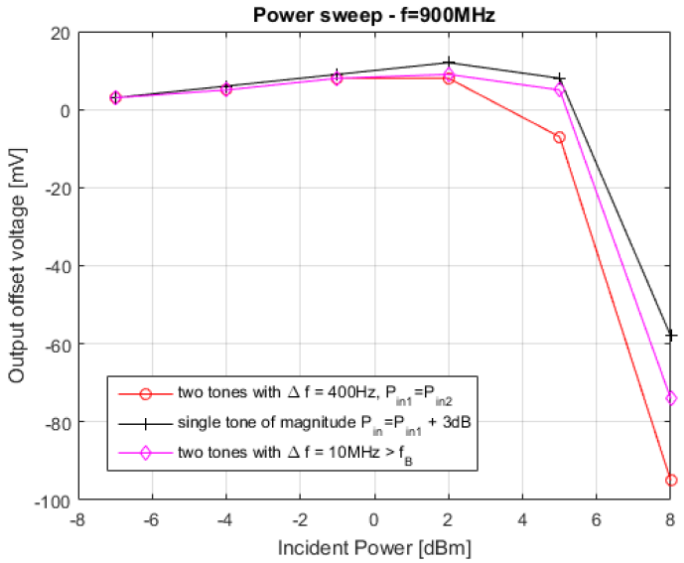


Figure 4.16: Measurements of the OpAmp output voltage offset induced by interference injection at 900 MHz.

Furthermore if the frequency spacing is within the OpAmp bandwidth, that is $\Delta f = 400\,\text{Hz}$ (red plots in Fig.4.14 to 4.16), also the beat appears in the output. The magnitude of the beat component is plotted in Fig.4.17 vs. the total injected power (sum of each tones contribution) for different carrier frequencies. It's evident that the amplitude of the beat component is actually higher than the offset induced by the same power CW interference, thus inducing failures that the CW would not. For example, suppose to qualify the OpAmp with a maximum power of 2 dBm and the susceptibility criterion to be an output voltage bounded by $\pm 200\,\text{mV}$. The IC will pass the DPI immunity test: the CW induced offset (black plots of Fig.4.14 to 4.16) is $\approx 100\,\text{mV}$ in the worst case. On the other hand, the same injected power will lead to a failure if the same power disturbance is split into two tones with frequency 100 MHz and spacing of 400 Hz. The amplitude of the beat component is indeed $\approx 300\,\text{mV}$ (red plot in Fig.4.17)

The injection of the two-tone interference with frequency spacing within the bandwidth of the DUT is a good solution to perform a wider-coverage qualification testing. It is especially useful in the case of circuit not affected by DC errors, thus supposed to be immune to EMI even if it is not.

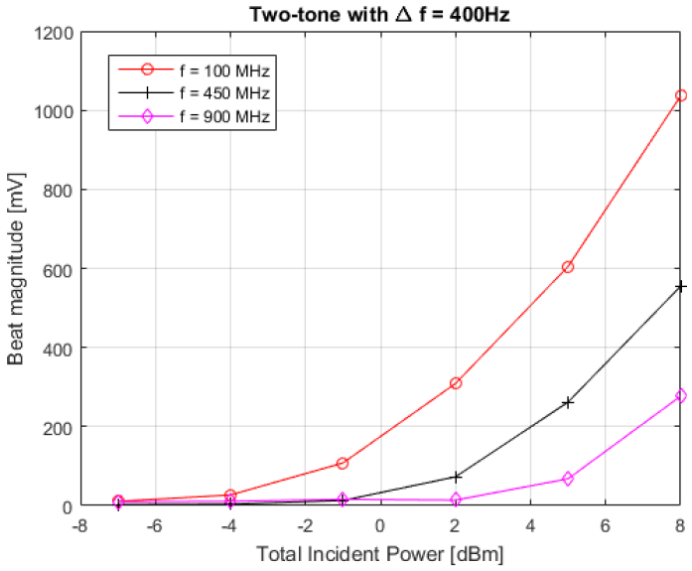


Figure 4.17: Measurements of the magnitude of the beat component induced by intermodulation distortion ($\Delta f = 400\,\mathrm{Hz}$).

Chapter 5

Susceptibility of 2.4 GHz Receivers to Low-Frequency Interference

A growing body of literature and researchers deal with the Internet of Things (IoT); such paradigm makes each connected object "smart" in the sense that everything can exchange information and make decisions based upon such information. For example a smart-home can decide to heat a place if the temperature is too low or switch-off lights in rooms where people have been moved through. IoT applications include not only home appliances, but also industrial automation, transportation and traffic control, smart grids, environmental monitoring and management. The number of connected appliances is expected to increase each year and predictions estimate that in 2020 there will be more than 200 billion of connected devices [39]. It is clearly a growing market segment, thus also an interesting research fields.

In the short-range, two wireless technologies arose as the main candidates for the IoT implementation, the Bluetooth Low Energy (BLE) and the IEEE 802.15.4 based equipment (e.g. the Zigbee protocol). They can be employed in the personal area networking or for wireless sensor network applications. Moreover, their low-power consumption makes them attractive for both portable and battery powered devices.

Both technologies, whose communication protocols are available on internet [40]-[41], operate in the 2.4 GHz license-free ISM band (from 2.4 GHz to 2.4835 GHz worldwide). These protocols specify the communication channel, the channel access method and the information encoding/decoding, basically the grammar and rules of a common language shared by the transmitter (TX) and the receiver (RX).

The main actor in the wireless communication process is the transceiver, a device capable of both transmitting and receiving information; the typical block diagram is depicted in figure 5.1. The receiving path is made by the antenna, the 2.4 GHz ISM Band-Pass Filter (BPF), the Low Noise Amplifier (LNA), the demodulator, the Analog to Digital Converter (ADC) and finally the digital core where the actual information is acquired. The incoming EM waves collected by the antenna are

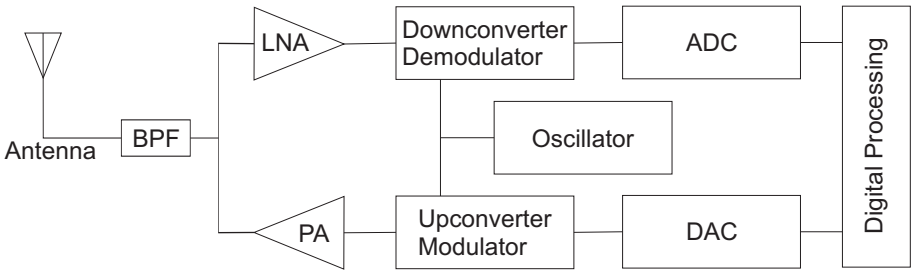


Figure 5.1: Block diagram of a generic RF transceiver.

first filtered to reject undesired signals, then amplified and demodulated to lower frequencies and finally converted and processed in the digital domain. On the other hand, there is the transmitter section, which is made by the digital processing that elaborates the information, the Digital to Analog Converter (DAC), the modulator and the Power Amplifier (PA). The information is encoded in the digital domain according to the communication protocol, converted into an analog signal, modulated and amplified to be finally transmitted by means of electromagnetic waves trough the antenna.

Most of the effort in designing 2.4 GHz ISM band transceivers is focused around the RF communication band. There are several tradeoffs to be taken into account: according to [42], they can be summarized in the design hexagon reported in figure 5.2. For example, to boost the gain of a LNA it is possible to increase the current flowing into transistors, thus raising the power consumption for a given supply voltage. At the center of the hexagon, figure 5.2, a new requirement has been introduced; the electromagnetic compatibility issue.

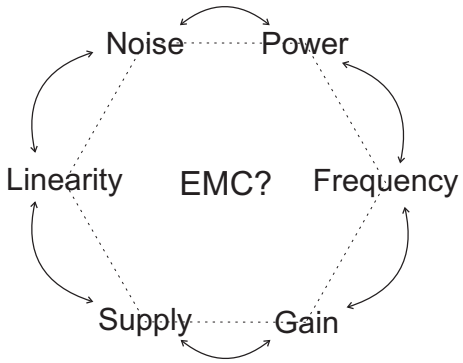


Figure 5.2: RF design trade-offs.

Radio equipment has to conform with normative and standards before being compliant, and thus sold. On one hand the receiver should acquire only the signal with frequency within the communication bandwidth and reject noise and unwanted

interference (RX should be almost immune to out-of-band EMI). The receiver should also work properly even in the presence of other appliances emitting in the same RF spectrum; several devices jammed the 2.4 GHz ISM band, not only Bluetooth and IEEE 802.15.4 but also Wi-Fi and microwave ovens. The coexistence of different devices sharing the same frequency band is therefore an issue. Nevertheless, several techniques have been developed to deal with it: subdivision of the communication band into several channels, the frequency hopping (TX and RX hops on different channels) or the carrier sense (if the wanted channel is idle, then transmit). They are useful to reduce the probability of collisions. On the other hand the transmitter shall radiates only in the chosen communication channel, most of the transmitted power should be bounded within the channel bandwidth (not to interfere with other equipment) and also the transmit time is regulated.

5.1 ETSI EN 300 328 and EMC Specifications

In Europe, the ETSI EN 300 328 [43] deals with radio equipment operating in the 2.4 GHz ISM band. The testing procedure are standardized to provide harmonized directives which conform radio devices. For example, the transmitter's output-power is regulated not only in its maximum but also in its frequency contents, within the communication band, out-of-band and in the spurious domain. These specifications can be summarized as depicted in figure 5.3, where BW is the bandwidth that contains 99% of the power of the signal being transmitted.

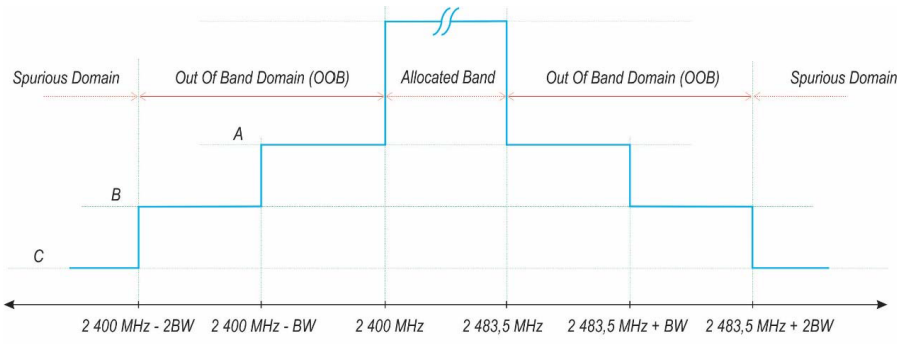


Figure 5.3: ETSI EN 300 328: TX emission in out-of-band domain.

Another example is given by the test setup for receiver blocking, depicted in figure 5.4. The wanted signal (green arrows) is fed to the chain by the signalling unit, i.e. a transmitter capable of connecting to the unit under test. The combiner adds together the wanted signal and the unwanted interference. Such interference (red arrows) is a Continuous Wave (CW) signal with specified frequency in the range 2300 MHz and 2673.5 MHz. The combined signal, which can be optionally checked

thanks to the directional coupler and the spectrum analyzer, is fed to the unit under test, that is the receiver. It shall exhibit a Packet Error Rate (PER) $\leq 10\%$ in the presence of unwanted signal.

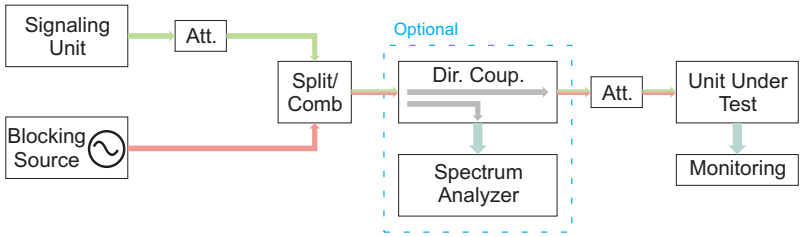


Figure 5.4: ETSI EN 300 328: set-up arrangement for testing the receiver blocking.

Also the BLE specification ([40]: Vol.6, Part A: section 4.2) deals with the interference performance of receivers. The wanted signal shall be a reference signal with power 3 dB above the receiver sensitivity. The interfering signal shall be a reference signal too; the frequency has to be within the 2.4 GHz-2.4835 GHz band and the power depends on the channel on which it is transmitted. For example, the power ratio between the wanted signal and the co-channel interference shall be of 21 dB. In the following section ([40]: Vol.6, Part A: section 4.3) the out-of-band blocking specifications are defined. The frequency range of the blocking signal is expanded with respect the ETSI EN 300 328, i.e. from 30 MHz to 12.75 GHz (excluding the communication band). The out-of-band suppression has to be measured with a wanted signal 3 dB above the receiver sensitivity and a CW interference with specified power (depending on the frequency range). For the lower-frequency range, i.e. 30 MHz to 2 GHz, the CW must have a power of -30 dBm. This specification states also that the receiver Bit Error Rate, which shall be $BER \leq 0.1\%$. Some exceptions (CW with frequency integer multiple of 1 MHz) are permitted.

Conversely, the IEEE Std 802.15.4 only specifies the rejection of an unwanted modulated signal on the adjacent and alternate channels (in-band interference). If the wanted channel is the number 7, then channels 6 and 8 are the adjacent channels while 5 and 9 the alternate ones. The Zigbee communication is based on the O-QPSK modulation, thus section 12.3.5 of [41](O-QPSK PHY RF requirements: receiver interference rejection) is referred. The test shall be performed with a wanted signal O-QPSK compliant and with a power 3 dB higher than the receiver sensitivity (at least -85 dBm). The receiver shall exhibit a $PER \leq 1\%$ when the O-QPSK compliant interference is applied. The power level of the disturbance in the adjacent (alternate) channel shall be 0 dB (30 dB) higher than the wanted signal power. Interference shall be applied one at a time.

5.2 2.4 GHz **Receiver**

The noisy environment imposes constrains on the design of transceivers and impacts directly the receiver sensitivity Sen. It specifies which is the minimum signal that can be successfully acquired in presence the noise:

$$Sen = \left(\frac{S}{N}\right)_{min} kTB\ NF \tag{5.1}$$

where k is the Boltzmann constant, T the temperature and B the bandwidth. $(S/N)_{min}$ is the minimum signal to noise ratio needed to acquire a signal. It basically sets a threshold in power between what is considered noise and what is the wanted signal. Finally, NF is the noise figure of the receiver defined as:

$$NF = \frac{SNR_o}{SNR_i} = \frac{S_o/N_o}{S_i/N_i} \tag{5.2}$$

where $SNR_x = S_x/N_x$ is the signal-to-noise ratio (subscripts i and o refer to the input and to the output respectively). This ratio is made in terms of average power in the communication band, S for the wanted signal and N for the noise. A receiver perform better if its sensitivity has lower values, indeed it can acquire signals with lower amplitude (thus the range of the communication can be increased). The parameter that has to be minimized in equation 5.1 is the noise figure of the receiver (for a given minimum detectable signal and bandwidth).

The noise figure of a receiving system made by cascaded blocks is given by the Friis formula:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \dots \tag{5.3}$$

where the increasing subscript refers to subsequent blocks in the chain. The receiver NF is minimized if the first block has a low-noise figure NF_1 and a high-gain G_1, i.e. if it is a Low Noise Amplifier.

In subsequent blocks the down-conversion is performed. Basically, there are two architectures: the homodyne (or direct receiver) which uses only one mixing stage to down-convert the wanted signal to base-band and to perform the quadrature demodulation. One block-diagram example is provided in figure 5.5. The heterodyne, on the other hand, uses two (or more) mixing stages as shown in the block diagram of figure 5.6. Another popular architecture, derived from the homodyne approach, is the low-IF architecture. The mixing frequency is chosen to down-convert the received signal to an Intermediate Frequency (IF) instead of the base-band directly.

The two architectures have in common the antenna, the communication Band-Pass-Filter (after the antenna) and the LNA. However, they impose different design tradeoffs, pros and cons: the homodyne has less stages (so less noise and power

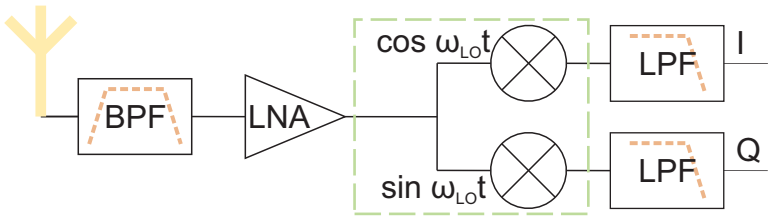


Figure 5.5: Architecture of a direct (or low-IF) receiver.

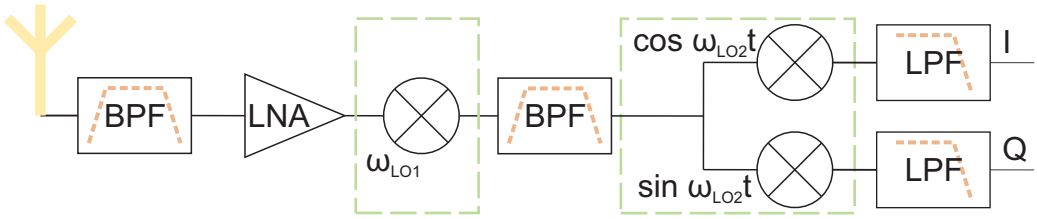


Figure 5.6: Architecture of an heterodyne receiver.

consumption) but suffers of oscillator leakage (receiver emits ω_{LO} through the antenna), DC offset (squared sinusoidal signal) and Flicker noise. The heterodyne, on the other hand has to face the problem of image (any signal with frequency components located around $\omega_{LO1} \pm (\omega_{LO1} \mp \omega_{ch})$ with $\omega_{LO1} \lesseqgtr \omega_{ch}$ where ω_{LO1} is the down-converting angular frequency and ω_{ch} is the channel center angular frequency). Such issue can be solved by filtering the output of the LNA (the BPF between the two mixing stages of figure 5.6) or by using architectures such as the Hartley or the Weaver one. The last architecture, i.e. the low-IF receiver, overcomes aforementioned limitations. The wanted signal is translated to an intermediate frequency rather than baseband, thus relaxing the DC offset and Flicker noise issues but also the image problem which can be filtered with the Low-Pass Filter LPF. The drawback of such architecture is that it requires an ADC working at higher frequency, thus with wider bandwidth (more power consumption) [42].

There are several topologies to down-convert and demodulate the received signal but they are not further investigated in this thesis. Indeed, if the LNA does not provide any useful signal, e.g. it switches-off, subsequent stages cannot work properly and the information cannot be successfully decoded. Moreover, the multi-standard transceiver used for testing allowed the comparison between two communication protocol running on "almost" the same hardware (BLE and Zigbee use a different number channels with different spacing and different modulations, thus the channel filter and the decoding differ). On the contrary, the two wireless technologies share the same communication band, so at least the antenna, the BPF filter, eventually a BalUn, and the LNA (see figure 5.1) can be the same for both protocols.

5.2.1 Low Noise Amplifier

In recent years, CMOS technology has grown in importance due to its low cost and to the opportunity of integrating the RF, analog, baseband and digital circuits within the same chip. There is a widespread body of literature that recognizes the importance of CMOS process in RF design [44]-[47]. Therefore two commonly used LNAs topologies (common gate and common source) were designed in 0.35 µm CMOS technology [29] and analyzed by means of Cadence [48]. The design was carried out to obtain a gain $\geq$15 dB and a good matching $S_{11} \leq -20$ dB in the communication band. Schematics comprise also protection diodes (1 kV human body model ESD) while the passive components (resistors, capacitors and inductors) were ideal to speed up simulations. LNAs were finally simulated with Spectre (a SPICE like simulator) to investigate their susceptibility to low-frequency interference applied at the input.

Common Gate with Cascode and Inductive Degeneration

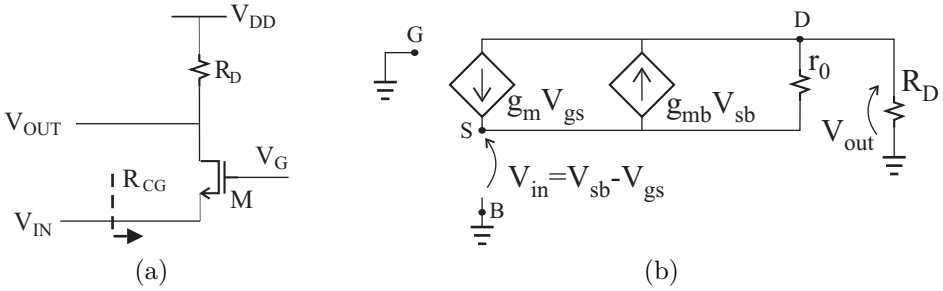


Figure 5.7: Common gate LNA schematic (a) and small-signal equivalent circuit (b).

The design of the Common Gate Low Noise Amplifier of Fig.5.7(a) can be started by matching the input impedance with the antenna (usually 50 Ω). The input resistance (and the voltage gain) of the CG-LNA can be calculated with the analysis of the small-signal equivalent circuit of a simple common gate as depicted in figure 5.7(b).

The input impedance is derived in appendix A.3 modeling the channel length modulation with r_0 and the body effect with the voltage controlled current source $g_{mb}V_{sb}$. It reads:

$$R_{CG} = \frac{R_D + r_0}{1 + (g_m + g_{mb})r_0} \tag{5.4}$$

The voltage gain V_{out}/V_{in}, see appendix A.4, is evaluated considering also the source

resistance $R_S = 50\,\Omega$.

$$A_V = \frac{(1 + (g_m + g_{mb})r_0)\ R_D}{r_0 + R_S + R_D + (g_m + g_{mb})r_0 R_S} \approx \frac{R_D}{2R_S} \tag{5.5}$$

The last simplification implies the matching condition of $1/(g_m + g_{mb}) = R_S$ and $r_0 \gg R_S + R_D$.

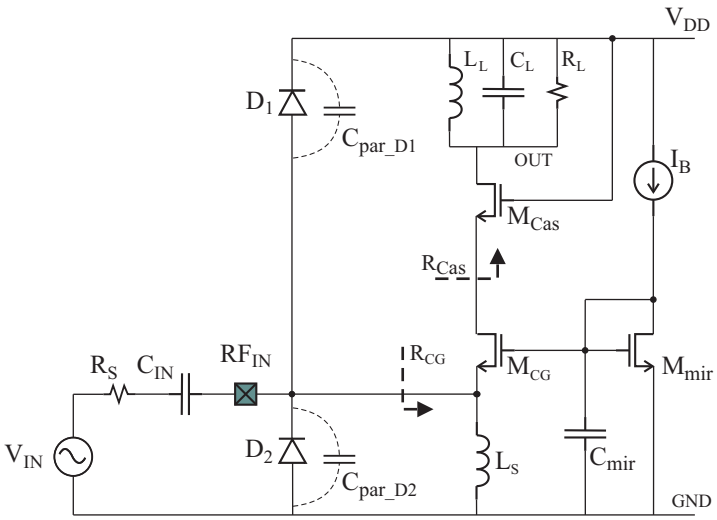


Figure 5.8: Designed Common Gate Low Noise Amplifier (CG LNA).

Cascoding the input transistor, see figure 5.8, both the input resistance and the gain change but they can be evaluated substituting R_D with the resistance seen at the drain of the input transistor R_{cas}. The input impedance of the overall stage is derived in appendix A.5.

$$R_{CG} = \frac{r_{0\_CG} + (g_m + g_{mb})_{Cas}\ r_{0\_Cas}\ r_{0\_CG} + R_L + r_{0\_Cas}}{[1 + (g_m + g_{mb})_{CG}\ r_{0\_CG}][1 + (g_m + g_{mb})_{Cas}\ r_{0\_Cas}]} \approx \frac{1}{(g_m + g_{mb})_{CG}} \tag{5.6}$$

The matching condition

$$\frac{1}{(g_m + g_{mb})_{CG}} = 50\,\Omega \tag{5.7}$$

can be accomplished by properly sizing the dimension of the input transistor M_{CG} and its drain current. Such high transconductance can be obtained by increasing the width of M_{CG} (thus reducing its transition frequency f_T) or by increasing the current (at the cost of higher power consumption). In the designed amplifier the transistor aspect ratio and drain current are chosen to be 150 µm/0.35 µm and 1.6 mA. The L_S inductance of 4 nH is chosen to resonate with the capacitance between the source node and ground. In this case it is dominated by the ESD parasitic capacitance $(C_{par\_D1} + C_{par\_D2})$.

As a first step, the dimensions of the cascode transistor M_{cas} can be chosen to be the same of M_{CG} and reduced afterwards to save area. Since its drain current is fixed, reducing the width of the cascode transistor too much will lead to higher gate-source voltage (V_{GS_Cas}), so less voltage headroom for M_{CG} to remain in saturation. In the designed amplifier $(W/L)_{Cas} = (W/L)_{CG}$. Finally, the $R_L L_L C_L$ tank is designed to resonate at the communication band center frequency; the inductance value is 5 nH while the added capacitance $C_L = 700$ fF goes in parallel with the M_{Cas} drain capacitance and eventually the input capacitance of subsequent blocks. The bias of the common gate input transistor is provided by the mirrored current source I_B.

The characteristics of the designed CG LNA are shown in Fig.5.11 with stars; the maximum gain (continuous line with stars) is ≈17 dB and it is possible to achieve a good matching, the simulated S_{11} (dashed line with stars) is lower than −30 dB.

Common Source with Cascode and Inductive Degeneration

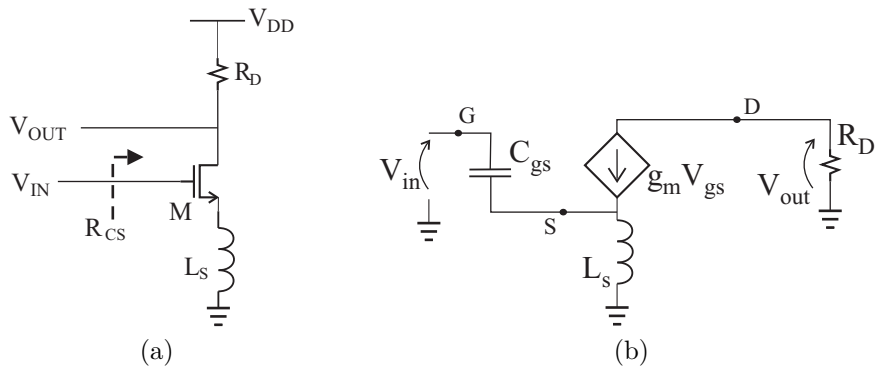


Figure 5.9: Common Source LNA schematic (a) and small signal equivalent circuit (b).

The input resistance seen at the gate of a common source MOS transistor is purely capacitive. The 50 Ω input matching can thus be accomplished by introducing the inductive source degeneration. Referring to the simplified schematic of Fig.5.9(a) and the small signal equivalent circuit of Fig. 5.9(b), the input impedance (see appendix A.6) can be evaluated as:

$$Z_{IN} = sL_s + \frac{1}{sC_{GS}} + \frac{g_m L_s}{C_{GS}} \quad \rightarrow \quad R_{IN} = \frac{g_m L_s}{C_{GS}} = 50\,\Omega \tag{5.8}$$

To directly compare the low-frequency behavior of the two topologies, the bias and dimensions of the input transistor are kept equal, that is $I_D = 1.6$ mA and $(W/L)_{CS} = 150\,\mu m/0.35\,\mu m$. Those parameters set also the transconductance g_m and the gate to source parasitic capacitance C_{GS}, thus fixing the inductance of L_s

for a given required matching. This value was too low, thus a capacitor of 140 fF was added between the gate and the source of M_{CS}, see Fig.5.10, with the aim of lowering the transistor f_T, thus increasing the inductance of L_S to 0.5 nH.

Moreover, the ESD protection diodes introduce a parasitic capacitance at the input node which lowers significantly the input impedance. A series inductor, as shown in the complete schematic of Fig.5.10, is used to counteract this unwanted effect ($L_G = 9\,\text{nH}$). The design has been completed by introducing the cascode transistor (with the same dimensions of the input one) and the $R_L L_L C_L$ tank: $L_L = 5\,\text{nH}$ and $C_L = 700\,\text{fF}$ as for the CG LNA. The bias of the input transistor is provided by the current mirror and the bias resistor $R_B = 600\,\Omega$; its value should be maximized to prevent further noise introduction [42].

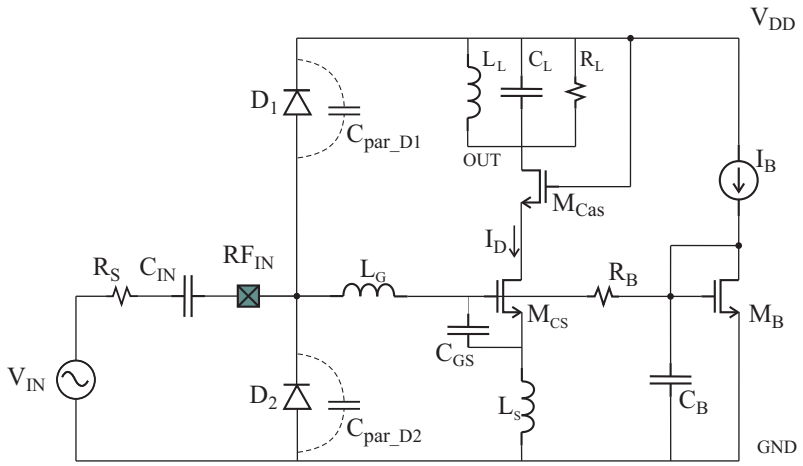


Figure 5.10: Designed Common Source Low Noise Amplifier (CS LNA).

The CS LNA, whose characteristics are outlined in Fig.5.11, presents a maximum gain of 24 dB (straight line) and an $S_{11} < -22\,\text{dB}$ in the communication band as shown by the dashed line.

The two LNAs are designed to keep the same transistor's bias and dimensions allowing a direct comparison between the topologies rather than optimizing them in terms of noise (figure 5.11 below). As expected the higher gain of the CS-LNA reflects in a lower noise figure. This is the reason why most of the designs employ the common-source topology (further enhancements can be the folded cascode [49], the differential signaling to cancel out common mode disturbance and second order non-linearities [50], the current reuse [51], the noise cancelation [52] or the forward body bias [53]).

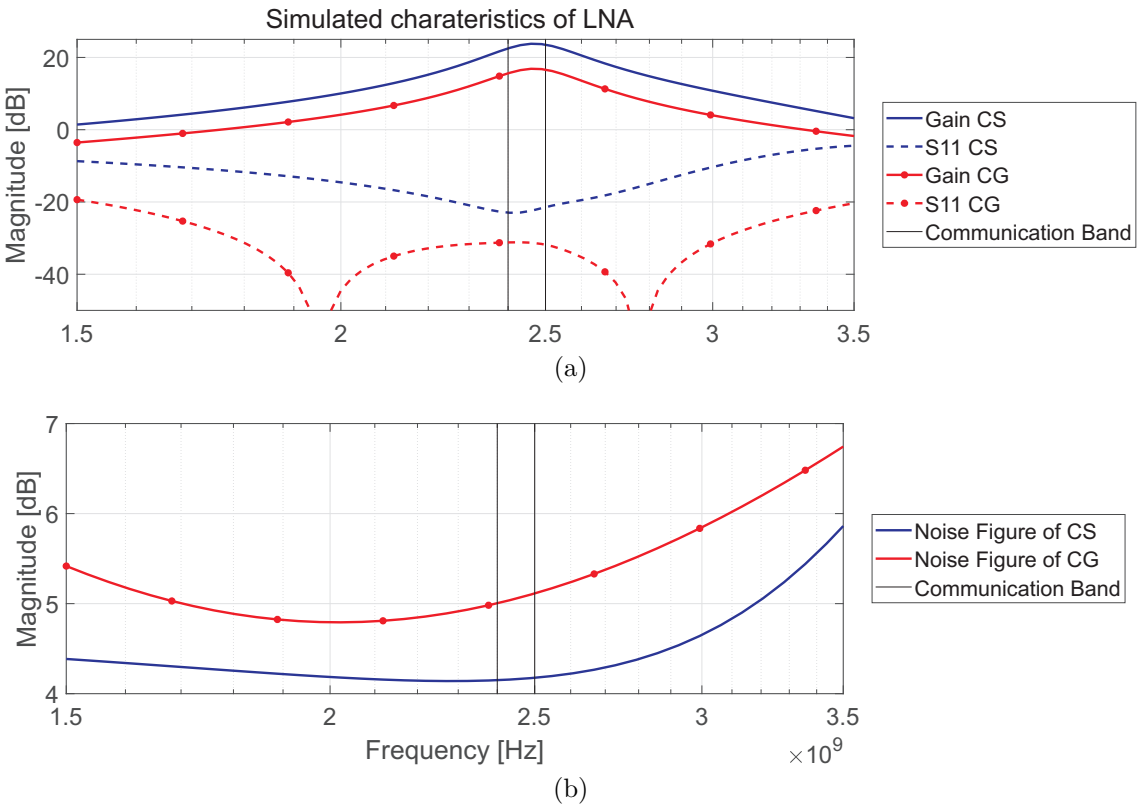


Figure 5.11: Simulated LNAs characteristics. Gain and S_{11} (a) and Noise Figure (b).

5.2.2 Susceptibility to Low-Frequency EMI

The susceptibility of the 2.4 GHz receiver to low-frequency interference was investigated focusing on the LNA and assuming a disturbance coupled onto the input pin. If the disturbance affects the ability of the LNA to propagate the wanted signal to the stages that follow, errors occur. This phenomenon surely takes place if ESD protection diodes (D_1 or D_2 in figure 5.8 and 5.10) conduct or if the input transistor leaves its nominal operating region (the former condition is strictly related to the second one).

The goal of the following analysis was to determine the amplitude of the interference that causes such events. The amplitude at the RF_{IN} input pin is determined by the injection circuitry and the low-frequency LNA impedance. Disturbance was applied by means of the voltage generator V_{IN} with the R_S =50 Ω reference impedance and a series decoupling capacitor C_{IN} big enough not to filter the input signal and thus relating simulation results with measurements presented in section 5.4.

The common gate topology (Fig.5.8) presents a low-frequency impedance dominated by L_S; by design it should resonates at 2.4 GHz with the capacitance existing between the transistor source node and ground. The inductor's value ranges in the nH and at low-frequency it behaves like a shunt to ground. This inductor together with R_S and the decoupling capacitor C_{IN} performs as a high-pass filter, which strongly attenuates low-frequency interference; this topology results to be very robust because disturbance does not interfere with the input transistor.

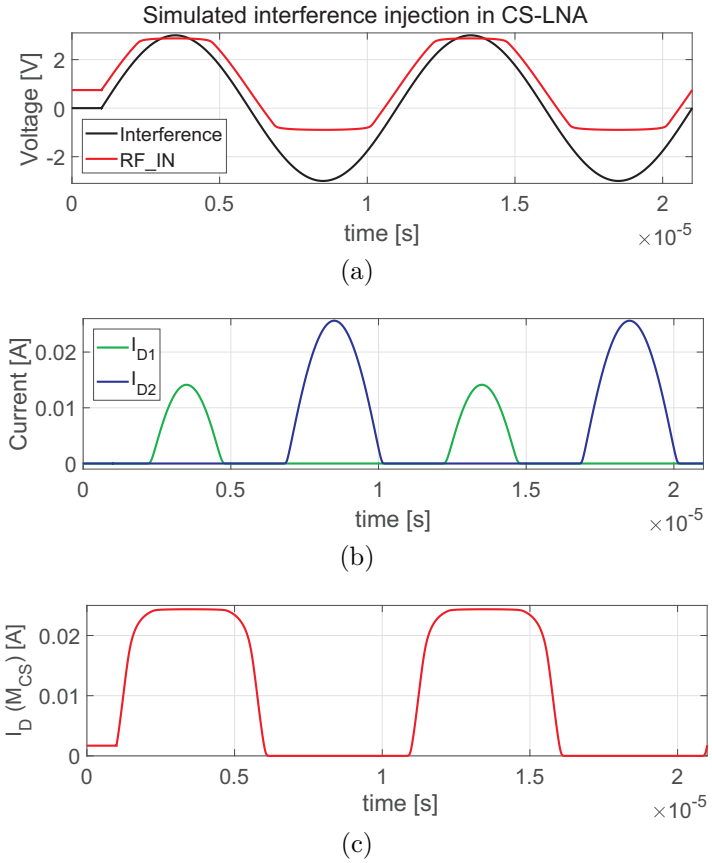


Figure 5.12: Simulation results highlighting the protection diodes conduction.

The CS-LNA (Fig.5.10), on the other hand, has a purely resistive low-frequency impedance determined by the series of the bias resistor R_B and the inverse of the mirror transistor transconductance $R_{CS} \approx R_B + 1/g_{m\_M_B}$. By design the value of R_B should be maximized, but a higher resistor will result in a worst filter attenuation (C_{IN} and R_{CS} act as high-pass towards the gate of M_{CS}). The amplitude of a low-frequency signal at the input pin (RF_{IN}) is then given by the voltage divider between R_S and R_{CS}. Moreover the RF input pin is kept at a constant DC voltage by the bias network, it equals the gate to source voltage $(V_{GS})_{M_{CS}}$, which should be

higher than the threshold voltage to have the transistor biased correctly.

An high amplitude signal at the receiver input can lead the ESD protection diodes D_1 (D_2) to conduct. If it happens, the received signal is shunted to the positive (negative) supply rail and the information cannot be decoded. Fig.5.12 refers to a simulation in which a sinusoidal voltage signal of 100 kHz frequency and amplitude of 3 V is injected, after an initial delay, in the CS-LNA input. When the voltage drop across the diode D_1 exceeds its threshold voltage V_γ, the diode enters in conduction (green line in Fig.5.12(b)). The RF_{IN} (and also the voltage at the gate of M_{CS}) clips at a voltage that is a threshold higher than the supply one (in this case 2 V + V_γ) and the input transistor is brought in triode. This phenomenon can be seen in Fig.5.12(c) where the transistor drain current is reported. Conversely, D_2 conducts for an input voltage lower than the diode threshold voltage (Fig.5.12(b) in blue). The input pin clips to $-V_\gamma$ (Fig.5.12(a) in red) and M_{CS} switches-off as can be seen from its drain current, Fig.5.12(c), which is 0 A.

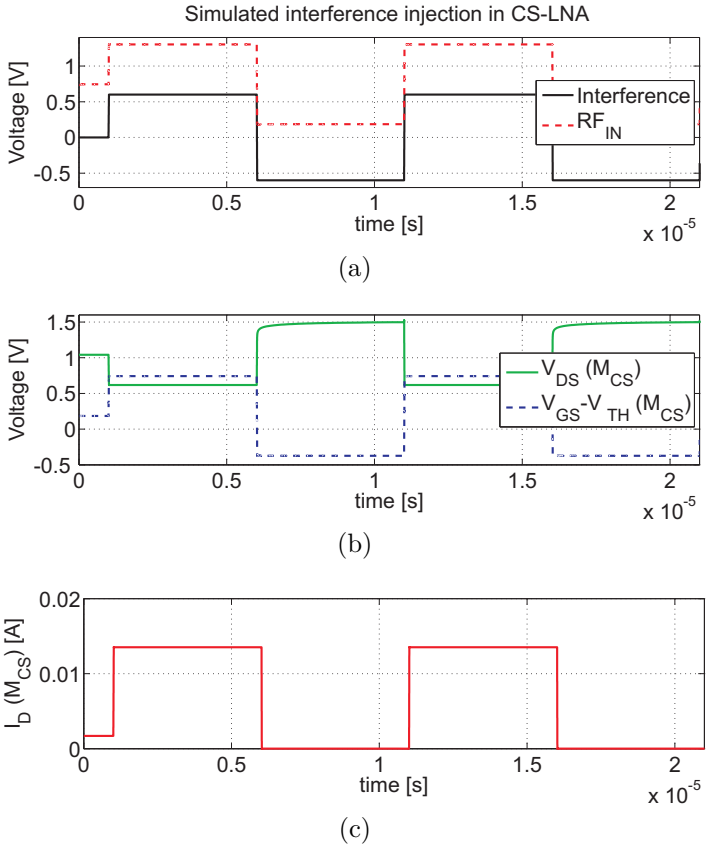


Figure 5.13: Simulation results for the square wave injection in the CS-LNA input.

Actually the input transistor of the CS stage will be driven in triode or switched-off even for lower-amplitude disturbance. Suppose the RF_{IN} voltage increases, the

drain current increases as well raising the gate to source voltage of M_{Cas}, which in turn lowers the V_{DS} of M_{CS}. For transistors of equal size (and neglecting the body effect) an input voltage $V_{RF_{IN}} > (V_{DD} + V_{TH})/2$ will drive the input transistor in triode, causing possible failures. Conversely, if the voltage at the RF_{IN} pin drops below the transistor threshold voltage, then M_{CS} will be switched-off. This last condition implies the lowest disturbance ensuring wrong LNA operation. A signal of amplitude greater than the transistor overdrive voltage $(V_{OD})_{M_{CS}} = (V_{gs}(t) - V_{TH})_{M_{CS}}$ superimposed onto the RF_{IN} input, will switch-off the input transistor each negative semi-period. The simulation results highlighting the above discussion are shown in Fig.5.13. After the initial delay a square wave of 100 kHz (Fig.5.13(a) in continuous line) is applied. The voltage at the input pin is the interference replica with lower amplitude and DC shifted (Fig.5.13(a), dashed line). In Fig.5.13(b) the drain to source voltage and $(V_{gs}(t) - V_{TH})_{M_{CS}}$ are reported with continuous and dashed lines respectively. This plot shows immediately when the transistor is in triode (continuous line below dashed one) and when it is switched off (dashed line below 0 V). This last condition can be double-checked with the drain current plot (Fig.5.13(c) in red). It is interesting to note that such a signal injected in the designed LNA will impair the reception of any wanted signal, thus any transmitted bit will be lost.

The input transistor of the CS-LNA can also be designed to work in moderate or weak inversion. For a give bias current it will have an higher transconductance, so the stage will have a higher gain and thus a better noise figure. The drawback is the reduction of the overdrive voltage and thus an increased susceptibility to low-frequency interference. The EMC-oriented characterization presented above has shown new tradeoffs in LNA design: the CG topology has lower gain (worse noise figure) but shunts low frequency interference coupled into the input pin. The CS counterpart has better performances in terms of gain and noise but is more susceptible to low-frequency interference. One way to increase the CS immunity is to design the transistor's dimensions and bias current to have an high overdrive voltage. It can be accomplished, for a fixed drain current, by decreasing the width (the length is usually the smallest possible depending on the technology). The transistor transconductance decrease as well, so the gain and thus also the noise figure worsens. Alternatively, the transistor aspect ratio can be kept constant and the drain current increased; in this way gain and noise figure get better but the stage consumes more power.

5.3 EMI coupling and propagation to the receiver input

The small form factor of RFIC allows transceiver to be embedded in system-in-package, e.g. three-dimensional 3D-IC, and almost in any PCB design. Environmental EMI can couple with the PCB antenna, traces or integrated inductors reaching the input of the LNA. A practical example is given in [54] where a switching DC-DC converter and a differential CS-LNA are stacked one above the other. The coupling mechanism was modeled from measurement results and the main contribution has been ascribed to the inductive coupling between the on-chip inductor of the DC-DC converter and the on-chip output inductors of the LNA. The same authors in [55] measure and analyze the coupling between the same DC-DC converter and a differential CG-LNA. In such experiment, the main inductive coupling mechanism pertains to the inductors used as source degeneration. The switched supply voltage of 3.3 V induces an interference amplitude of ≈80 mV (worst case) across such inductors. This coupled interference can alternatively switch-off input transistors if their designed overdrive voltage is lower than this value but authors focused more on the LNA output rather than the inputs.

EMI can couple also with PCB traces or antennas, propagating through the band-pass filter and thus reaching the input of the LNA, causing eventually upset in the communication. This phenomenon is analyzed considering practical PCB printed antennas and the BPF+BalUn of the unit under test.

5.3.1 Coupling with PCB printed antennas

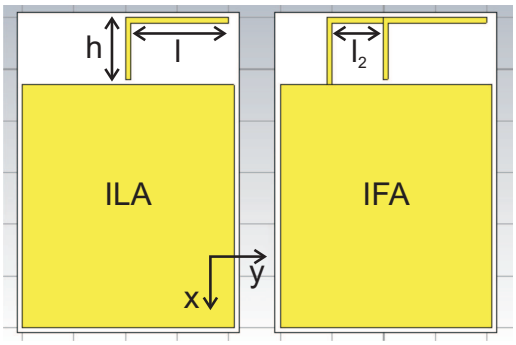


Figure 5.14: PCB printed antennas geometry.

PCB printed antennas are copper traces drawn directly on the dielectric layer of the printed circuit board. In the 2.4 GHz ISM band, the corresponding wavelength is $\lambda \approx 12.5$ cm, thus $\lambda/4$ antennas are relatively compact in size and can be printed

on the same transceiver PCB. Furthermore, PCB antennas are easy to manufacture and cheap, still providing good performances.

Two practical antennas (see Fig.5.14) were considered: the Inverted L Antenna (ILA), which is a monopole antenna bent of 90°, and the Inverted F Antenna (IFA), which is an ILA with a stub shorted to the ground plane. The simulated PCB (about 4 cm×5 cm) was made up of FR-4 of thickness 0.73 mm. The ground plane and the antennas were drawn with a pure copper layer. The dimensions of the ILA are: height $h = 1$ cm, length $l = 2$ cm and width of 1 mm. The IFA, for a direct comparison, is made equal to the ILA and a stub to ground is added at a distance of $l_2 = 1$ cm. For both the antennas the feed point was kept 1 mm away from the ground plane. The interference source was supposed to be a cable (modeled as a pure copper cylinder) running in the y direction above the antenna longer arm. This wire had radius of 1 mm, length of 8 cm and a variable distance d (in the z direction) from the PCB plane. The full structure simulated is presented in Fig.5.15 and 5.18 for the ILA and the IFA respectively. Simulation are performed with CST Studio Suite [56], in particular CST Microwave Studio and CST EM Studio are used for the antenna design and the simulations. The transient solver is based on the finite integration method and it works on hexahedral grids with adaptive mesh refinement. Each simulation requires 3 consecutive cycles to obtain the required accuracy of −60 dB and lasts approximately 11 h-13 h to be completed.

The circuit under analysis is also analyzed analytically. Since it is several order of magnitude smaller (electrically short) with respect to the smallest wavelength in the frequency range considered (up to 1 MHz $\rightarrow \lambda = 300$ m), it can be modeled as lumped elements. The main coupling mechanism is analyzed by simplifying the geometry of the problem to parallel wires.

Inverted L Antenna

The inverted L antenna at low frequency is basically an open circuit behaving like a capacitor. Its equivalent impedance Z_{ILA} can be derived from the simulated S_{11} showing a capacitance of about 750 fF. Thus the capacitive coupling is expected to be the main contribution and it has been also highlighted by simulations. The simulated coupling, indeed, depended only on the voltage signal, being independent of the current flowing in the cable.

Simulations were carried out having the ILA and the ground plane above and below the FR-4 layer as shown in Fig.5.15. The coupling between the wire and the antenna can be modeled as a parasitic capacitance C_{par} between the interferer wire and the antenna feed point. The distance of 1 cm gave raise to $C_{par} = 220$ fF; the increased distance (d has been changed to 1.5 cm, 2 cm and 4 cm) implied less coupling, indeed $C_{par} \approx 175$ fF, 150 fF and 145 fF, respectively.

The inspection of the geometry has led to some simplifications in order to treat

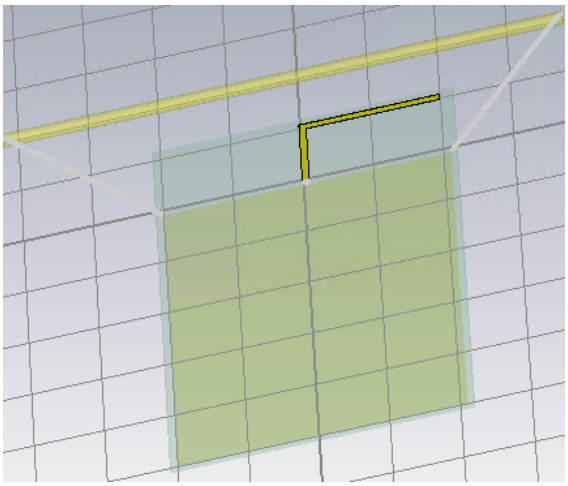


Figure 5.15: ILA full structure used for simulations.

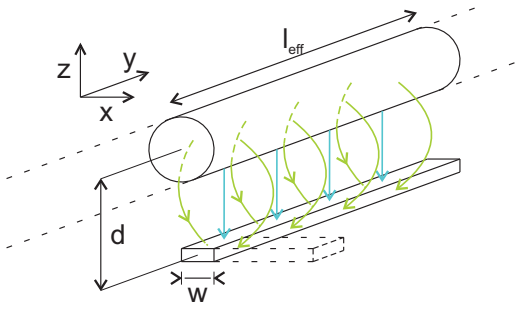


Figure 5.16: Simplified geometry for the mutual capacitance evaluation.

the problem analytically. First the presence of the dielectric layer and of the ground plane were neglected, thus the greater contribution was expected to be due to the wire and the antenna. The geometry simplification is depicted in Fig.5.16 where the effective length is $l_{eff} = l = 2\,\text{cm}$ (antenna longer arm). The parasitic capacitance describing the main coupling mechanism resulted to be the one between the cylinder (with radius of r_w =1 mm) and the long flat brick ($w = 1\,\text{mm}$)

Since the two charged objects are parallel the first assumption that comes into mind is to consider them as parallel plates. Such assumption, however, will lead to an underestimation of the capacitance, indeed it does not consider the fringing effect (bent arrows) but only the electric field lines perpendicular to the plates (straight vertical arrows in Fig.5.16). The last simplification, owing to the brick geometry and the small width compared to the length, was to consider it as another cylinder of radius equal to $r_{mod} = w/2$. In this way all the electric field lines were taken into

account and the mutual capacitance between the two wires became

$$C_{par} \approx \frac{2\ \pi\ \epsilon_0\ l_{eff}}{ln[d^2/(r_w\ r_{mod})]}. \tag{5.9}$$

The modeled capacitance and the simulation results are plotted in Fig.5.17 with continuous line and stars respectively. Although a lot of simplifications, the calculated parasitic capacitances and the simulated ones match well. The analytical model of Eqn.5.9 can be useful since it relates directly the parasitic capacitance with the cable and trace dimensions and their distance.

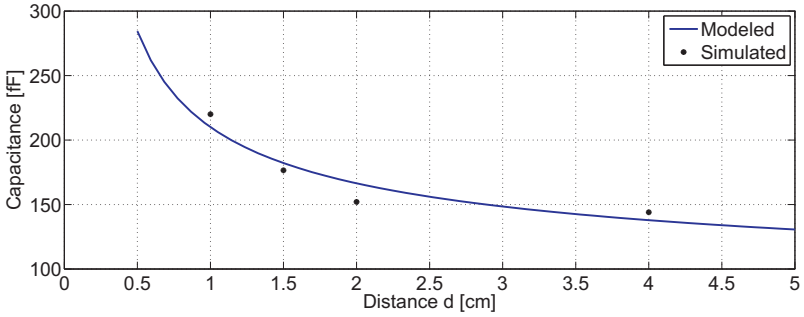


Figure 5.17: Parasitic capacitance modelling and simulations (full structure).

Inverted F Antenna

The inverted L antenna, on the other hand, is basically a short circuit at low frequency: the simulated equivalent impedance is an inductance of about 25 nH. For a direct comparison with the ILA, the wire was parallel to the antenna longer arm and moved in the vertical direction, see Fig.5.18. The simulated coupling, in this case, depends mainly on the current signal flowing in the wire suggesting an inductive coupling. The wire-antenna mutual inductance was estimated directly from the simulation results; it equals 4.4 nH, 3.9 nH, 3.7 nH and 3.5 nH for d =1 cm, 1.5 cm, 2 cm and 4 cm, respectively.

The mutual inductance can also be derived analytically simplifying the structure to a three parallel wires. The first is the actual interferer wire, the second is the receptor wire (the antenna) and the third is the return current carrying wire (the ground plane). The greater coupling contribution was supposed to take place in the short-stub, indeed it forms a square loop which collects the magnetic flux ψ. The simplified geometry resulted to be the one depicted in Fig.5.19 where $l_{eff} = l_2 = 1$ cm is the short-stub length. The mutual inductance, according to [14], was evaluated considering the magnetic flux ψ_w and ψ_{GND} generated by the current i_G flowing in the interferer wire and returning through the ground plane.

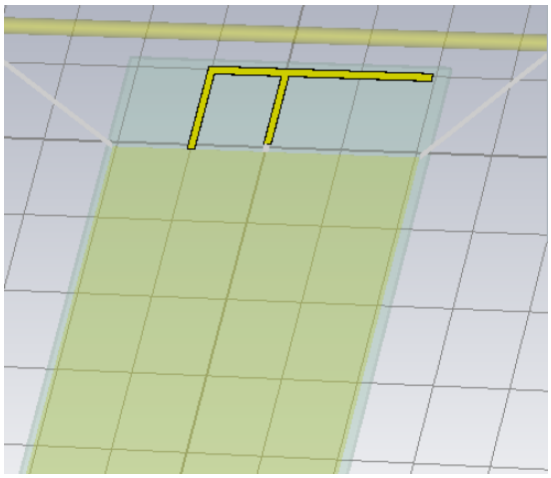


Figure 5.18: IFA full structure used for simulations.

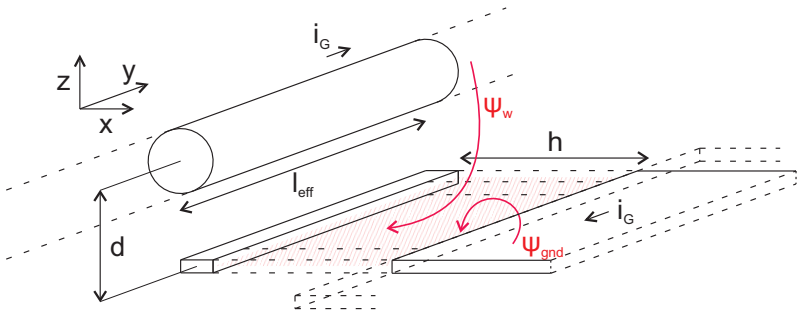


Figure 5.19: Simplified geometry for the mutual inductance evaluation.

The analysis led to the following expression:

$$L_m = \frac{\psi_w + \psi_{GND}}{i_G} \approx \frac{\mu_0 \, l_{eff}}{2 \, \pi} ln \left(\frac{\sqrt{d^2 + h^2} \, h}{d \, r_{GND}} \right) \tag{5.10}$$

where r_{GND} is the radius of the wire that can be used to model the ground plane. This equivalent radius is chosen to be the same of the interferer wire radius, that is $r_{GND} = r_w = 1\,\text{mm}$. The calculated mutual inductance (red dashed line in Fig.5.21) overestimates of about 1 nH the simulated one (black stars) but, despite that, this simplified model can be used to evaluate the order of magnitude of the mutual inductance. Simulation results can be fitted by increasing the equivalent radius: ψ_{GND} lowers and consequently also the mutual inductance decreases. The physical explanation is that the returning current in the reference plane is not confined by geometrical constraints (contrary to the wire and the copper trace) and spreads more in the x-direction.

In the last approximation a new model has been derived in order to fit the

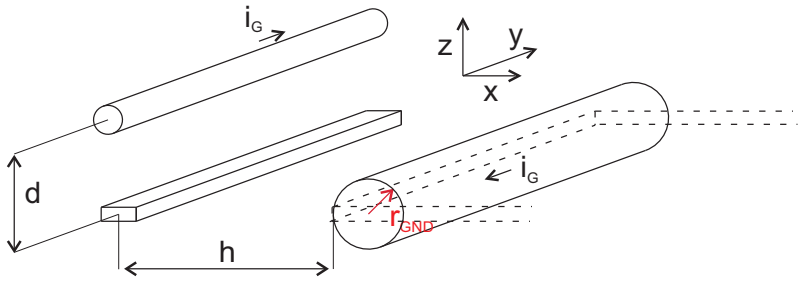


Figure 5.20: Modified geometry for the mutual inductance evaluation.

simulation results. Fig.5.20 shows the modified geometry highlighting the wire used to model the ground plane contribution. Eqn.(5.10) become:

$$L_m \approx \frac{\mu_0 \, l_{eff}}{2 \, \pi} ln \left(\frac{\sqrt{d^2 + (h + r_{GND})^2} \, (h + r_{GND})}{d \, r_{GND}} \right) \tag{5.11}$$

and the evaluated mutual inductance is plotted in Fig.5.21 with the green line. The good agreement with simulation results indicates that the return current distribution in the vicinity of the antenna should be carefully investigated.

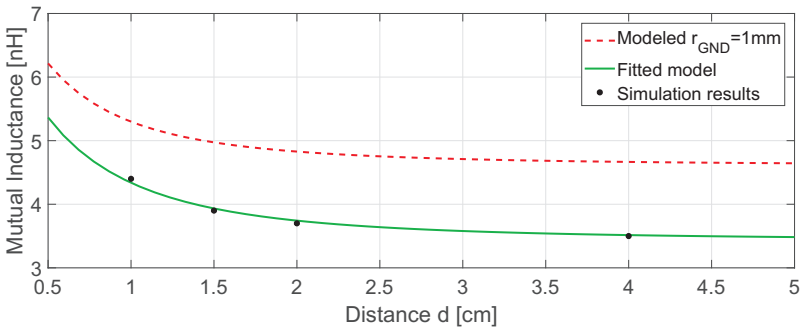


Figure 5.21: Mutual inductance modelling and simulations (full structure).

5.3.2 Propagation in the Front End

The propagation of disturbance to the receiver input pin is analyzed referring to the device under test [57]. The PCB front-end schematic is presented in Fig.5.22: from left to right on the PCB there are the SMA connector used to connect the network analyzer, the LC band pass filter, the LC BalUn used for the differential signaling and the RFIC. The low frequency path from the input capacitor to the RF_n input allowed the receiver input impedance measurement. The series capacitor C_{IN}

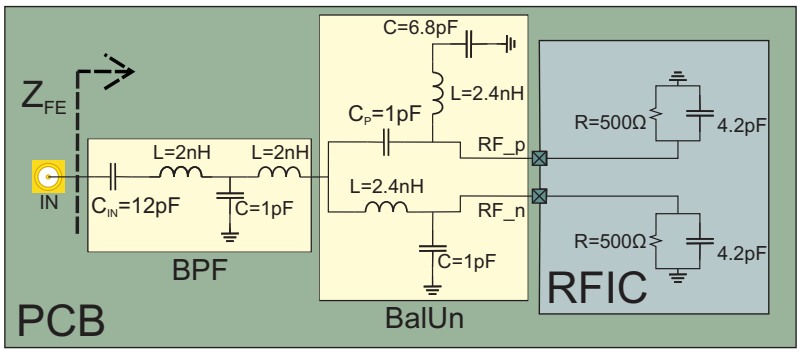


Figure 5.22: Schematic view of the Front-End of the RF receiver under test.

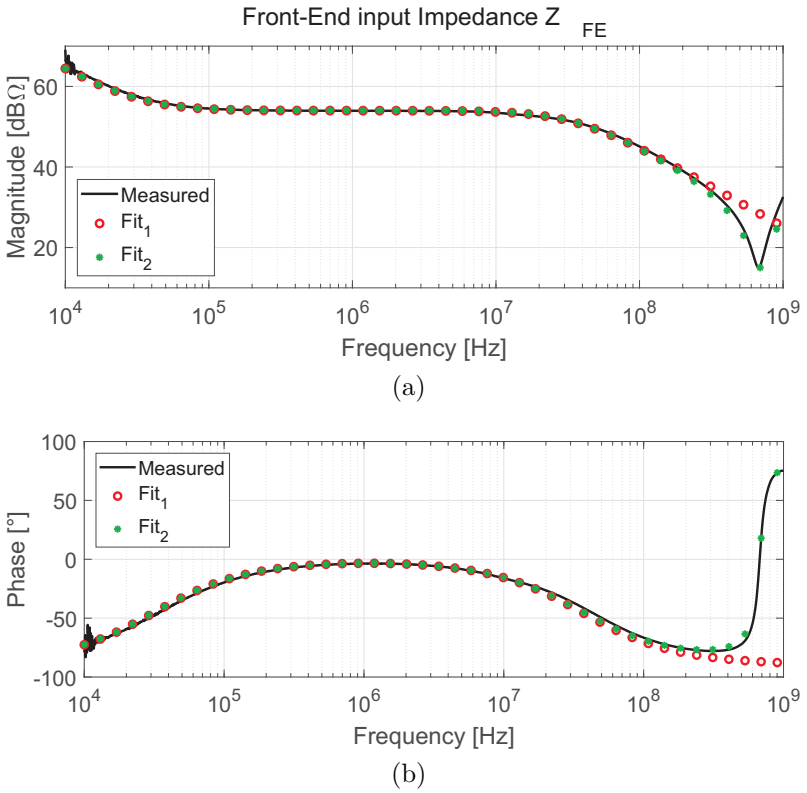


Figure 5.23: Measured and modeled Front-End input impedance in magnitude (a) and phase (b).

shall be increased and the transceiver (running the BLE or the Zigbee stack) set in receiving mode.

Plots in Fig. 5.23 show the measured low-frequency Front-End impedance Z_{FE} (in black) with $C_{IN} = 10\,\text{nF}$ and two fittings (green stars and red circles). The receiver impedance at low frequency is resistive ($\approx 500\,\Omega$) up to several MHz; the

capacitance introduced by the BPF, the BalUn and the two inputs causes the first pole. Z_{FE} can be fitted (red circles) through

$$Fit_1 \rightarrow \frac{1}{sC_{IN}} + R//\frac{1}{sC} \tag{5.12}$$

where $R = 500\,\Omega$ and $C = 8.8\,\text{pF}$. At higher frequency also inductances play a role. The resonance at 670 MHz can be modeled (green stars) adding a series inductance as done in

$$Fit_2 \rightarrow \frac{1}{sC_{IN}} + sL + R_{ser} + R//\frac{1}{sC} \tag{5.13}$$

where $L = 6.4\,\text{nH}$ and $R_{ser} = 4\,\Omega$. The low-frequency impedance of the RFIC input was evaluated de-embedding previous results, thus obtaining a resistance in parallel with a capacitance. R is approximately $500\,\Omega$ and $C \approx 4\,\text{pF}$ as shown in Fig.5.22 within the grey box. This capacitance is probably introduced by the parasitics of input pads, RF switch and ESD protection circuits but also an integrated capacitor can be used for matching.

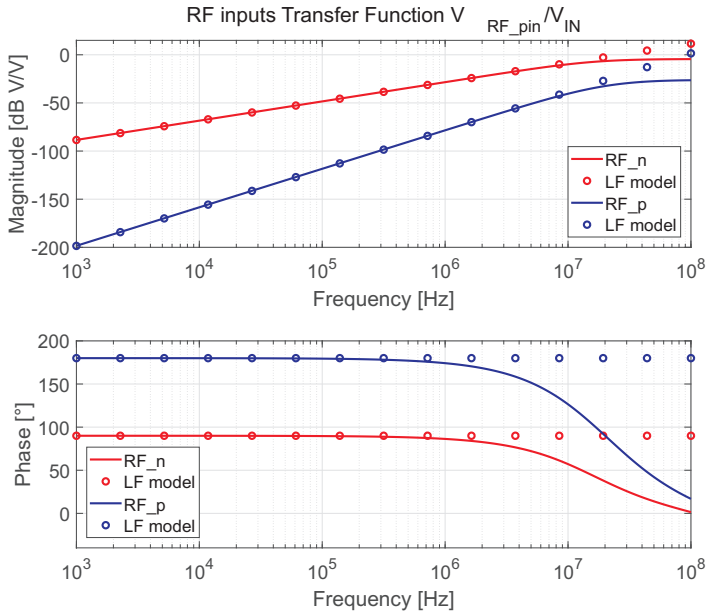


Figure 5.24: RF inputs transfer function, V_{RF_pin}/V_{IN}.

The low-frequency disturbance at the RX input pins is determined by the coupling mechanism, the BPF+BalUn design and by the receiver low-frequency impedance. The transfer function from the injection point to the receiver inputs can be evaluated and simulated once the RX impedance is known. At low-frequency (below 100 MHz) all the inductors are basically shorts and they can be omitted. From

circuit inspection, the RF_n input results to be high-passed once while RF_p is further high-passed thanks to the C_P series capacitor of the BalUn. The transfer functions results to be:

$$\frac{V_{RF\_n}}{V_{IN}} \approx \frac{j\omega RC_{IN}}{j\omega R(C_{IN}+C_{EQN}+C_P)+1} \approx j\omega RC_{IN} \tag{5.14}$$

being $C_{EQN} \approx 6.2\,\text{pF}$ the equivalent capacitance existing between the RF_n node and ground. The pole has cut-off frequency of about 16 MHz.

$$\frac{V_{RF\_p}}{V_{IN}} \approx V_{RF\_n}\frac{j\omega RC_P}{j\omega R(C_P+C_{EQP})+1} \approx -\omega^2 R^2 C_{IN} C_P \tag{5.15}$$

where $C_{EQP} \approx 11\,\text{pF}$ is the equivalent capacitance of the RF_p pin. This high pass filter introduces another pole at $\approx 26\,\text{MHz}$. AC simulations of the complete Front-End are plotted in Fig.5.24 with continuous red line for the RF_n input and in dashed blue line for RF_p. The approximations in (5.14) and (5.15) are plotted with circles. They are well suited for signals of frequency lower than 1 MHz.

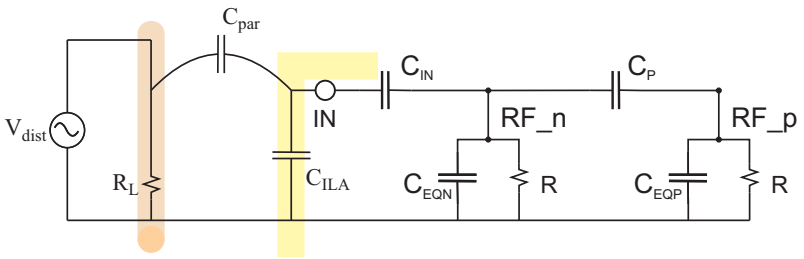


Figure 5.25: Schematics for the received disturbance evaluation (capacitive coupling).

The reduced schematic is plotted in Fig.5.25 and Fig.5.26; inductors were removed and capacitors in parallel gathered into the equivalent capacitors. The Front-End schematic is also fed by the coupling equivalent model and loaded with the antenna low-frequency equivalent impedance.

In Fig.5.25, the capacitive coupling of the Inverted L Antenna is modeled by the parasitic capacitance C_{par} connected between the disturbance voltage source V_{dist} and the injection point IN. The Front-End is also loaded with the antenna impedance C_{ILA}, which is purely capacitive in the frequency range considered. At low-frequency the voltage disturbance is propagated through the series of the parasitic capacitance and the input capacitor, which basically equals the parasitic capacitance. Up to 1 MHz the received voltage can be simplified to:

$$\frac{V_{RF\_n}}{V_{dist}} \approx j\omega RC_{par} \qquad \frac{V_{RF\_p}}{V_{dist}} \approx -\omega^2 R^2 C_{par} C_P. \tag{5.16}$$

The received capacitively-coupled voltage is plotted in Fig.5.27 with red and blue continuous lines for the RF_n and RF_p inputs respectively. The parasitic capacitance reduces the transfer function (see Fig.5.24) of about 34 dB and moves the pole at higher frequency. The voltage resulting at the RF_n (RF_p) pin raises of 20 dB (40 dB) per decade up to the pole frequency. The approximations of (5.16) are plotted in Fig.5.27 with stars. They match simulation results (both in the magnitude and in the phase) for interfering signals of frequency lower than 1 MHz.

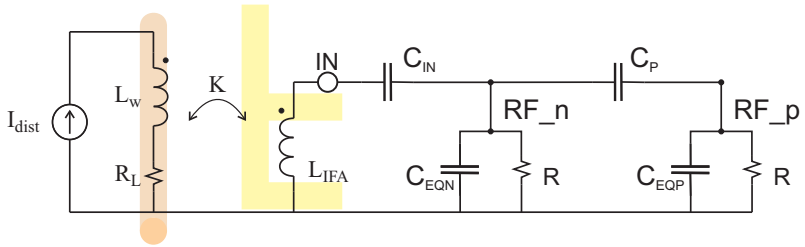


Figure 5.26: Schematics for the received disturbance evaluation (inductive coupling).

On the other hand, the inductive coupling of the inverted F antenna can be modeled as two coupled inductors (Fig.5.26) where $L_W = 3.7\,\text{nH}$ is the wire simulated inductance and L_{IFA} the antenna low-frequency inductance. The coupling coefficient K can be expressed as

$$K = \frac{L_m}{\sqrt{L_w\ L_{IFA}}}. \tag{5.17}$$

Under the assumption of weak-coupling, the source current I_{dist} induces a voltage across L_{IFA} given by $V_{IN} = j\omega L_m I_{dist}$. The received inductively-coupled voltage can thus be expressed as

$$\frac{V_{RF\_n}}{I_{dist}} \approx -\omega^2 L_m R C_{IN} \qquad \frac{V_{RF\_p}}{I_{dist}} \approx -j\omega^3 R^2 L_m C_{IN} C_P. \tag{5.18}$$

In Fig.5.27, dashed black and green lines represent the simulated received voltage at the RF_n and RF_p inputs respectively. At low-frequency, the voltage at the RF_n pin increases of 40 dB intercepting the received capacitive-coupled voltage around 670 kHz. The approximation of (5.18) is showed with stars and it is in good agreement with simulation results up to 1 MHz. As expected the low-frequency path from the antenna to the RF_n input pin makes this node subjected to higher amplitude interfering signals. The RF_p input is further high-pass filtered, so that interference are more attenuated.

The receiver transfer function simplification, see (5.16) and (5.18), and the coupling models, (5.9) and (5.11), can be used to derive the CW interference amplitude

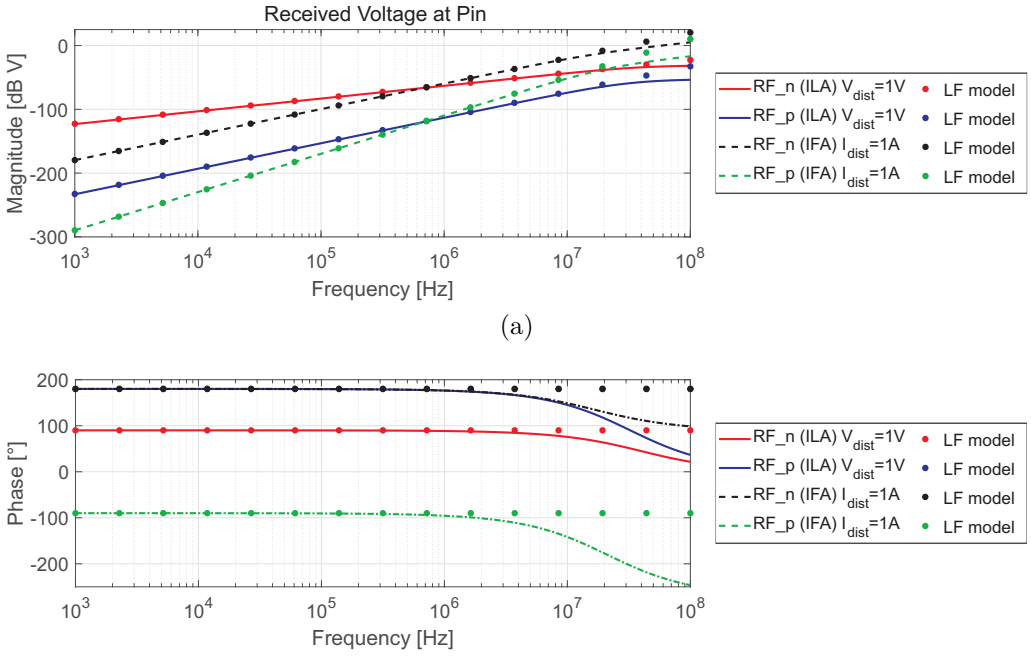


Figure 5.27: Simulated (and modeled) disturbance received at Pin. Magnitude (a) and phase (b).

needed, e.g., to have 1 V at the RF_n input pin as shown in Fig.5.28. The simplification is valid only for low-frequency interference but it is of particular interest since the receiver under test was found to be particularly susceptible to injected disturbance having frequency lower than 1 MHz.

For the Inverted L Antenna a voltage disturbance of 15 kV to 1.5 kV of amplitude in the nearby wire will give rise to a 1 V coupled signal. The same received voltage will be induced by the coupling of a high current (10 kA to 1 kA) flowing in the wire near the Inverted F Antenna at least in the 300 kHz-1 MHz frequency range.

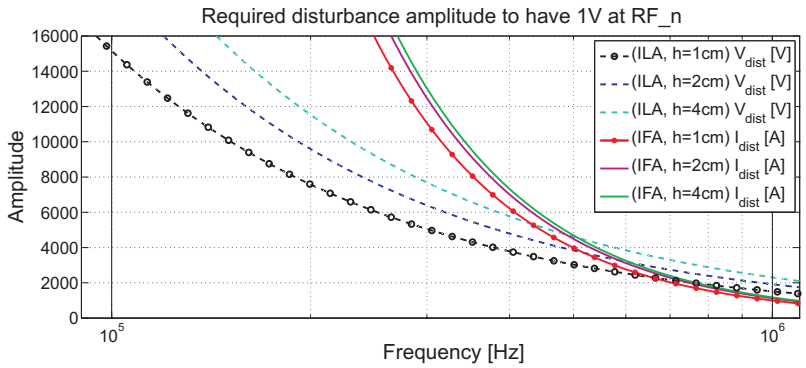


Figure 5.28: Comparison between the simulated couplings.

5.4 Low-Frequency susceptibility measurements

The susceptibility of 2.4 GHz receivers to low-frequency disturbance has been evaluated by means of several measurements. The multi-standard transceiver under test [57] is depicted in Fig.5.29. The PCB of the evaluation board comprises the Inverted F Antenna, the 2.4 GHz Band-Pass Filter (BPF), the BalUn and the Radio Frequency Integrated Circuit (cc2650 SimpleLink Multistandard MCU). This control unit contains a 32-bit ARM Cortex-M3 processor and several peripherals. The transceiver is compatible with Bluetooth Low Energy 4.2 and IEEE 802.15.4 specifications. The radio controller is embedded into the read-only-memory and partly running on a separate ARM Cortex-M0 processor. As can be seen in Fig.5.29 (orange box), it is possible to solder an SMA connector and bypass the PCB printed antenna by moving the input capacitor of the BPF (C_{IN}) through the SMA trace. This operation allowed firstly the measurement of the receiver input impedance and secondly the injection of the low-frequency interference directly in the receiver input.

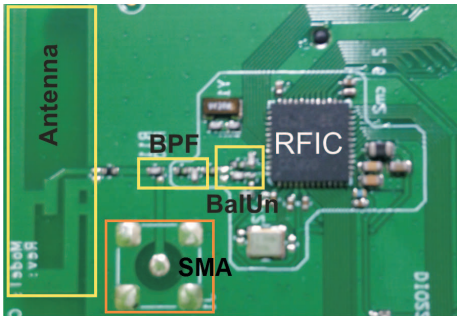


Figure 5.29: Photograph of the transceiver under test.

The test setup arrangement used for the interference injection is schematized in Fig.5.30 and it is rather similar to the Direct Power Injection method. The

PC has been used to control, via GPIB (red dashed line), the signal generator, namely the frequency, the amplitude, the waveform type, the start and the stop of the disturbance injection. The PC controlled also the two evaluation modules (highlighted with green dashed lines) running the native PER test. The SmartRF Studio software has been used to set up of the main radio communication parameters: the communication protocol, the transmitter output power, the channel and the number of packets being sent (the transmitter will send 100 equal packets every 60 ms). The receiver, on the other hand, was supposed to acquire all the packets on the same communication channel outputting on the PC all the received ones, even with errors, and the packet Received Signal Strength Indication (RSSI).

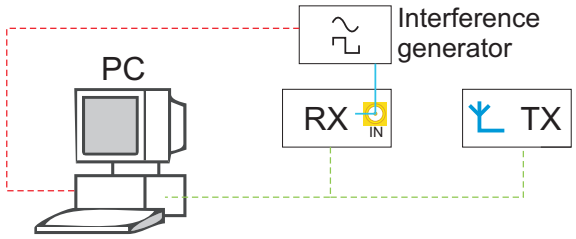


Figure 5.30: Measurement setup used for the analysis of the low-frequency susceptibility of RF receivers.

The transmitter output power, the distance and the orientation of the two modules were adjusted in order to ensure first a wireless communication without error (all the sent packets are correctly received) with controlled packet RSSI. Afterwards the interference is injected in the receiver input and the received data saved for the post-processing. One example is given in Fig.5.31; it refers to the injection of a 500 kHz square wave of amplitude 0.5 V in the differential transceiver running the IEEE 802.15.4 compliant stack.

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11:50:50.794 | 0011 | 8d c3 ac bf ce b9 e3 10 38 a2 ee e1 39 89 bc 2d 6c ed e1 11 0d 66 a1 8b af 8c 4a 82  | -87
11:50:50.864 | 0012 | 8d c3 ac bf ce b9 e3 10 38 a2 ee e1 39 89 bc 2d 6c ed e1 11 0d 66 a1 8b af 8c 4a 82  | -88
11:50:50.934 | 0007 | 27 c3 ac bf ce b9 e3 10 38 a2 ee e1 39 89 bc 2d 6c ed e1 11 0d 66 a1 8b af 8c 4a 82  | -88
11:50:51.004 | 0014 | 1d c3 0c 1f ce b9 e3 10 38 a2 ee e1 39 89 bc 2d 6c ed e1 11 0d 66 a1 8b af 8c 4a 82  | -88
11:50:51.074 | 0015 | 8d c3 ac bf ce b9 e3 10 38 a2 ee e1 39 89 bc 2d 6c ed e1 11 0d 66 a1 8b af 8c 4a 82  | -88
```

Figure 5.31: Example of errors induced by interference injection.

As highlighted with red circles the packet number 13 and the following one are received with errors. In the first packet both the sequential number and the first octet are wrongly decoded while in packet number 14 the least significant 4 bits of the first, third and fourth octets of the payload were wrongly decoded. Data were acquired and post-processed analyzing the sequential number and the payload. If the received packets has at least one error in such fields, then it will be considered wrong. The reasoning led to a modified PER definition to account also all the

packets lost:

$$PER = \frac{100 - P_{ok}}{100} \tag{5.19}$$

where P_{ok} is the number of all correctly received packets.

Summarizing, the constant received packet RSSI was used to arrange both the transmitter output power and the position in order to ensure an error-free wireless communication while the PER has been adopted as susceptibility metric. The measurement technique is rather simple and can be performed with minimal hardware; it only requires a transmitter, a receiver and a low-frequency signal generator.

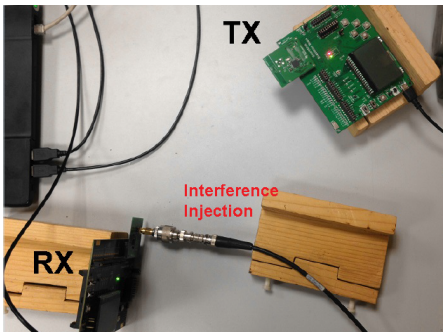

Figure 5.32: Photograph of the measurement setup for the RF receiver susceptibility evaluation.

Preliminary susceptibility evaluation

In the first measurement session the input capacitor of 12 pF was changed to 10 nF. The Agilent 33120A Function/Arbitrary Waveform Generator has been used as interference source varying the waveform, the frequency and the amplitude of the injected disturbance. The averaged received-packet RSSI was set at ≈−80 dBm and several measurements were made varying the distance (≈25 cm to 30 cm) and the orientation of the two modules, see Fig.5.32. This photo shows the transmitter (TX), the receiver (RX) and the interference injection path through the SMA connector.

Fig.5.33 collects the measurements results for all the waveforms provided by the generator: the sawtooth wave, the square wave and the sinusoidal wave. The sawtooth wave has been injected with a maximum amplitude of 500 mV and varying the frequency from 1 kHz to 100 kHz because of limitations of the signal generator itself. It induced a maximum PER of about 25%.

The sinusoidal waves have been injected varying the frequency from 1 kHz to 1 MHz and the amplitude until the interruption of the communication has been registered. The 200 kHz interference broke the communication for the maximum amplitude of 1.5 V.

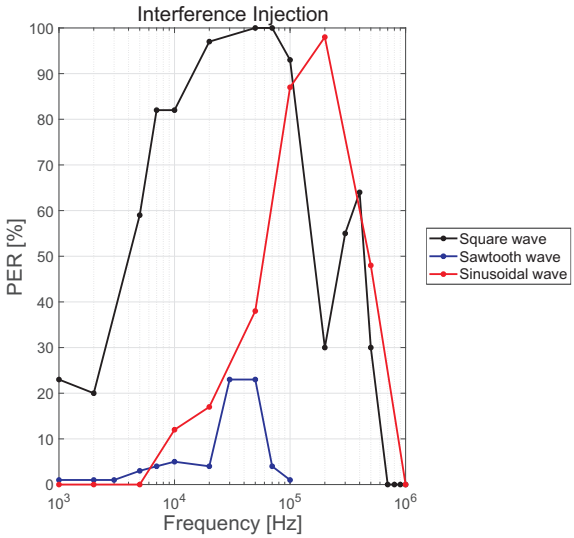

Figure 5.33: Preliminary measurement results for different interfering waveforms.

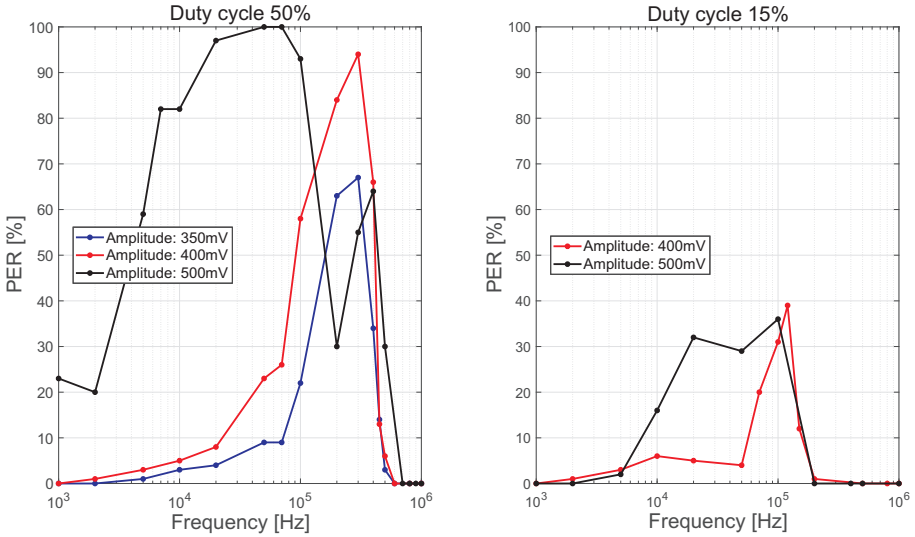

Figure 5.34: Measurement results for different duty cycle.

The same procedure was repeated for the square wave changing the frequency from 1 kHz to 1 MHz (the maximum allowed by the signal generator) and increasing the amplitude. It has been noticed that an amplitude of 500 mV (three times lower than the sinusoidal wave) was enough to induce relevant errors (more than 90% of the sent packets were not correctly received). The effects arising from the injection of the square wave were then investigated changing also the duty cycle.

In Fig.5.34 on the left there is the evaluated PER for an injected square wave

of amplitudes 350 mV (in blue), 400 mV (in red) and 500 mV (in black), with duty cycle of 50%. The frequency was spanned from 1 kHz to 1 MHz. The two lower-amplitude waveforms cause the highest errors (PER>20%) in the 100 kHz to 400 kHz disturbance frequency range with a peak at 300 kHz for both. At this frequency the communication is practically lost (PER>90%) for the 400 mV square wave amplitude. The 500 mV square wave will cause more errors in a larger frequency range. The PER is greater than 20% in almost the whole frequency range (no errors was observed for interference with frequency >500 kHz and the communication can be considered broken for disturbance frequencies in the 20 kHz to 100 kHz range (PER higher than 90%). The plot in the right of Fig.5.34 refers to the evaluated PER for an injected square wave with lower duty cycle (15%). At a glance errors are strongly reduced and the receiver is immune to the disturbance of 350 mV of amplitude. Errors are reduced by one third, that is the same ratio between the two duty cycles.

5.4.1 Differential receiver

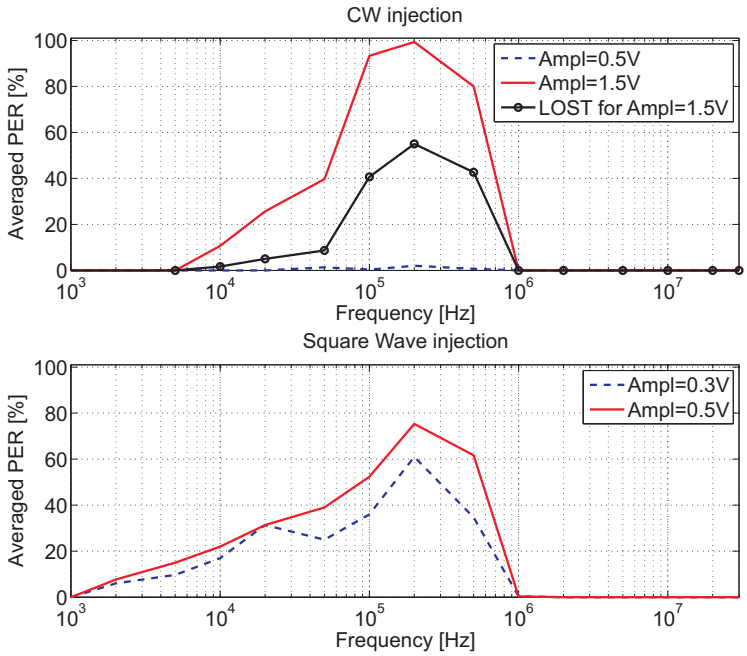

Figure 5.35: Measurement results of session #1.

In the measurement session #1 the input capacitor is kept 10 nF: low-frequency disturbance reaching the RF_n pin will be partially filtered, indeed signals were high-passed once (the pole is at about 30 kHz). The signal generator has been changed (Stanford Research System DS345 function generator) to inject as well

higher frequency square waves. The frequency span is enlarged from 1 kHz to 30 MHz, thus covering all the frequencies excluded by the BLE out-of-band blocking specification (which is the more stringent specification for 2.4 GHz receivers).

Three channels (3, 27 and 39) were tested first ensuring an error-free communication (≈ -83 dBm of packet RSSI) and then injecting the disturbance (only the CW signal and the square wave). The registered errors are averaged and the resulting PER is reported in Fig.5.35. For all channels the receiver is very susceptible for interference signals having frequency within the 100 kHz-1 MHz range and practically half of the packets were lost (line with circles) for the highest amplitude CW signal.

This first measurement session (but also the preliminary one, see Fig.5.33) has shown that the receiver is almost immune to the square wave disturbance with frequency $\geq$1 MHz. It means that are not the high frequency contents of the signal that induce upset in the receiver but rather the positive semi-period of the interfering waveform. Comparing Fig.5.35 and Fig.5.33 it is possible to state that errors depends not only on the power of the received signal (in this session it is reduced and the same interference induces more errors) but also on the time in which the receiver input transistors are perturbed. Reducing this period of time by reducing the duty cycle has led to less errors.

Session #2

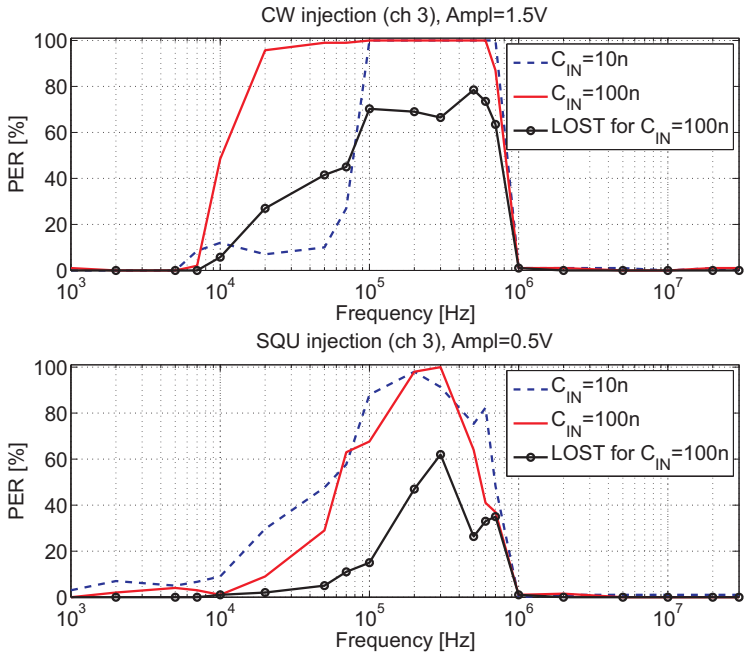

Figure 5.36: Measurement results of session #2.

In the session #2, measurements were first repeated focusing only on the communication channel 3 and fixing the orientation of the two modules (facing each other at a distance of 40 cm). Adjusting the transmitter output power, the packet RSSI was set at about −90 dBm. The evaluated PER is in Fig.5.36 in dashed blue lines.

Next, the input capacitor was changed again to 100 nF (the pole moves to 3 kHz). The PER and the number of lost packets are reported in Fig5.36 with the continuous red line and black line with circles respectively. Errors increase in the lower frequency range for the CW injection only; the square wave causes approximatively the same errors for both configurations. Far more packets are lost in the 100 kHz-1 MHz frequency range. Again the receiver proves to be very robust for disturbance with frequency higher than 1 MHz.

5.4.2 Single-ended receiver

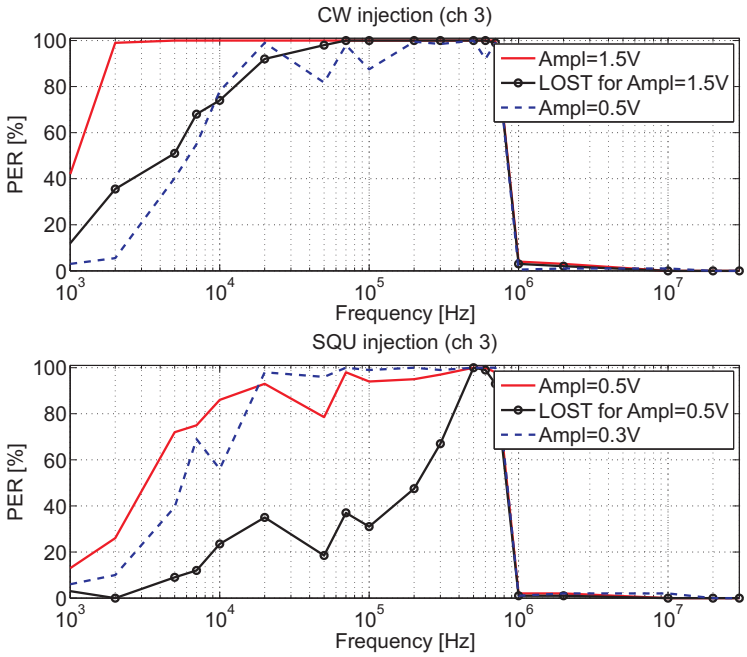

Figure 5.37: Measurement results of session #3.

In the third session the receiver was made single-ended removing the RF_p series capacitor. The position and the received power were the same of measurement session #2. As can be seen from the PER reported in Fig.5.37 the receiver is completely desensitized for a CW disturbance of 1.5 V amplitude (straight line) loosing all packets (circles) in the 100 kHz-1 MHz frequency range. At lower frequency, more packets were received but most of them with errors. Even the 500 mV amplitude CW

interference (dashed line) will practically block the communication if its frequency is between 10 kHz and 1 MHz (the Packet Error Rate is greater than 80%).

The injected square wave interference will block the receiver if the frequency is within 20 kHz-1 MHz (continuous and dashed lines). The number of lost packets (compared with the differential configuration, see Fig.5.36) is significantly higher: more than 20 from 10 kHz and practically all in the range 500 kHz-1 MHz.

Single-Ended Receiver, Low-Amplitude

In the last set of measurement (session #4) the susceptibility of the receiver was tested with signals having amplitudes of 100 mV and 200 mV. As can be seen in Fig.5.38, most of the errors are located in the 10 kHz-1 MHz frequency range for both the disturbance waveforms. There is a maximum around 500 kHz where the square wave injection (continuous red line) breaks the communication. On the other hand, the CW induces only a PER>40% (dashed line). The receiver seems to be immune to the lowest amplitude injected interference (green line with circles), only five received-packets were wrong for the square wave with frequency 500 kHz.

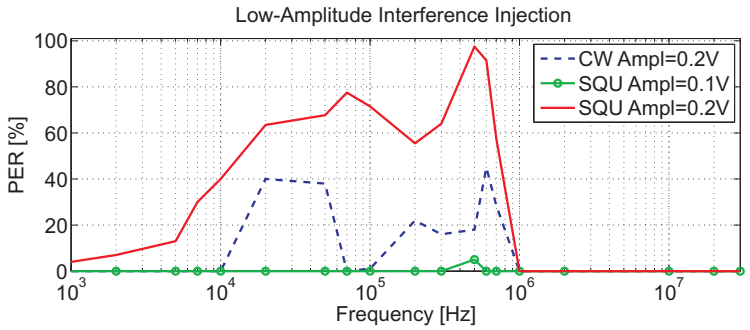

Figure 5.38: Measurement results of session #4, low-amplitude interference.

5.4.3 Comparison between BLE and Zigbee

The measurements of session #3 and #4 were repeated with the aim of comparing the BLE communication and the IEEE 802.15.4. For both protocols the received-packet RSSI has been set to −90 dBm and the center frequency (2410 MHz) of the communication channel is chosen to be the same; BLE communicated on channel 3 while the Zigbee channel was the number 12. Fig.5.39 shows the evaluated PER referring to the injection of a square wave with amplitude 300 mV and 500 mV. The frequency spanned the 1 kHz-30 MHz range.

As it can be seen, the Zigbee receiver was completely desensitized (PER > 80%) by disturbance with frequency in the 5 kHz-50 kHz range. Higher frequency interference, between 300 kHz and 1.2 MHz, induced remarkable errors especially for the

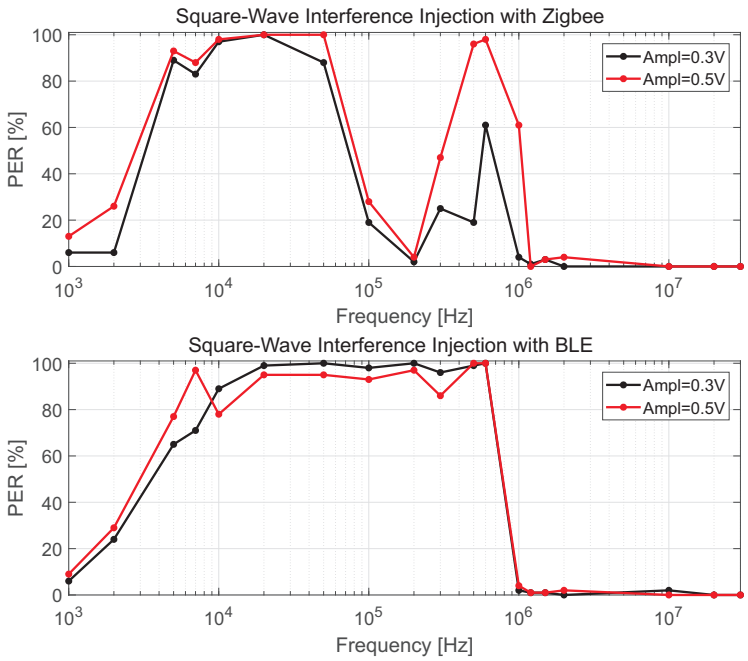

Figure 5.39: Measurement results of session #5.

higher amplitude. On the other hand, the BLE receiver showed a PER >80% for injected interference with frequency within the 10 kHz-1 MHz range (in accordance with results of Fig.5.37).

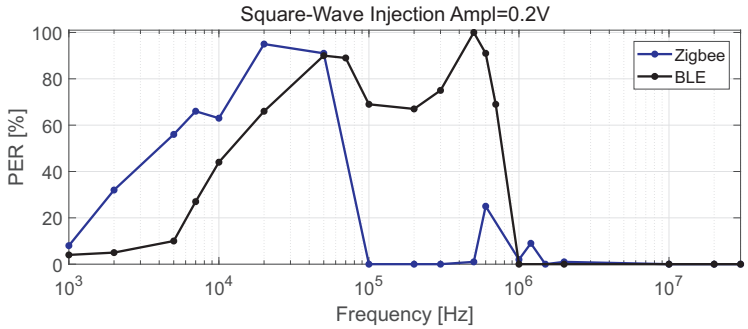

Figure 5.40: Measurement results of session #5, low-amplitude interference.

The receiver showed errors even with lower-amplitude square waves (i.e. 200 mV). As can be seen in Fig.5.40, most of the errors were located in the 10 kHz-1 MHz frequency range for the BLE communication (black line) while the Zigbee was more susceptible to disturbance with frequency lower than 100 kHz as shown by the blue line.

5.5 Discussion

The measured low-frequency input-impedance of the receiver under test suggests that a CS LNA is employed. It relates the measurements to the analysis of Section 5.2.1. Results presented in Fig.5.38 and Fig.5.40 showed significant errors for an interference signal with 200 mV amplitude (comparable with transistor overdrive) and the complete blocking of reception for higher amplitude injected signals (Fig.5.37 and Fig.5.39). The reason of the observed failures can be ascribed to the time in which the input transistor is switched off, that is at least one interference semi-period (see Fig.5.13).

Dealing with the BLE communication, the bit period is $T_B = 1/BR_{BLE} = 1\,\mu s$ and if the input transistor does not propagate the wanted signal for at least this period of time, errors certainly occur. Such reasoning is consistent with the frequency range in which the receiver is more susceptible, that is 100 kHz-1 MHz, where the interference semi-period is comprised between $5T_B$ and $0.5T_B$. It also explains the fact that the BLE communication is always lost for a square wave of frequency 500 kHz (for which the interference semi-period equals the bit period) and the immunity of the receiver to interference with frequency $\geq$1 MHz.

The differential operation of the receiver partially alleviates such problem especially in the lower frequency range: one input is further high-pass filtered, thus low-frequency interference is more attenuated and the received signal can be decoded. Nonetheless, even with the differential operation the receiver shows relevant errors in range 100 kHz-1 MHz. Moreover, the reduction of the time in which the input transistors were disturbed (by the reduction of the duty cycle) has shown benefits in the communication (see Fig.5.34) with a reduction in the number of errors proportional to the duty cycle reduction.

The same reasoning applies also to IEEE 802.15.4 based communication. In this protocol 4 information bits are spread on a sequence of 32 chips, then even (odd) indexed chips are modulated onto the in-phase (quadrature-phase) carrier and finally transmitted with a chip rate of 2Mbit/s (the O-QPSK symbol rate is 62.5ksymbol/s). Thus the receiver has 16 µs to decode a symbol but if the LNA does not propagate the signal for this period of time (square wave of frequency $\leq$ 31.25 kHz), errors surely occur.

Measurement reported in Fig.5.39 showed relevant errors also for an injected square wave with frequency around 500 kHz (from 300 kHz to 1 MHz). The receiver, thus, seems to suffer the perturbation induced by the interference having the semi-period equal to the actual bit-period but further considerations can be made only knowing the actual receiver design and architecture.

In Section 5.3 it has been shown and modeled the main coupling mechanism

between a source of interference and the antenna. Two practical PCB printed antennas, the Inverted L and the Inverted F, were designed and simulated. The interferer considered was a cable suspended above the PCB at a variable distance; it has made possible the derivation of an analytical model and a lumped-element equivalent circuit describing the capacitive (inductive) coupling of the ILA (IFA). The propagation to the receiver inputs has been analyzed using the band-pass filter and the BalUn of the RF module under test [57]. The coupling mechanism and propagation is analyzed and simplified for interference with frequency lower than 1 MHz, indeed measurement results do not show relevant error for higher frequencies. Even if it is not generalizable for all receivers, it is a useful starting point in understanding the fundamental circuit behavior and to highlight design tradeoffs. For example, a CW voltage (current) of frequency 600 kHz and amplitude of ≈ 500 V (≈ 550 A) on the wire 1 cm distant from the ILA (IFA) will lead to a 200 mV received disturbance at the RF_n input pin. Such disturbance will cause a PER larger than 40% on the single ended receiver running the BLE stack (Fig.5.38). On the other hand, a triangular voltage wave of frequency 600 kHz and amplitude 2 kV on the wire near the ILA will be translated into a square wave of amplitude $\approx$530 mV at the RF_n input (the transfer-function shows a derivative behavior). Such interference interrupts completely both the BLE and the Zigbee communications (Fig.5.39).

Conclusions

Despite decades of investigations the EMC issue is an ongoing research field, and it is critical for IC reliability. In this thesis the EMC of Operational Amplifiers has been reviewed dealing in particular with the Direct RF Power Injection method. The susceptibility of such building block is analyzed and evaluated by measurements referring first to the standardized injection of CW signals. A method to model the DPI set-up with the aim of analyzing the interference propagation in modern ICs is proposed and the EMIRR has been questioned. Such parameter is basically a small signal parameter, useful only in predicting the offset induced by small-amplitude interference, thus having limited validity.

The natural progression was to analyze feedback OpAmps subjected to multi-tone interference, indeed the CW approach is not really suitable to reproduce actual EM disturbance. An analytical model has been derived to predict the offset induced by multi-tone interference with frequency spacing greater than the bandwidth of the amplifier and also the amplitude of the beat component induced by the application of a two-tone interference. The intermodulation distortion has been also investigated by means of measurement results on commercially available OpAmps and an affordable test set-up is also proposed to cover this new susceptibility criterion.

The EMC of 2.4 GHz receivers has been also questioned in the low-frequency range owing the fact that practical switching circuit generates interference with frequency components below the minimum frequency defined in specifications (i.e. 30 MHz). Disturbance, indeed, can couple from an electromagnetic polluted environment and propagate to the receiver inputs. Low-frequency interference with high-enough amplitude can periodically switch off the LNA input transistors, and thus such building block cannot propagate the wanted signal to the stages that follows. If this phenomenon lasts longer than a symbol period, then the reception will be surely upset. Disturbance with higher amplitudes can lead ESD-protection diodes in conduction, and then the reception will be impaired as well. A low-frequency immunity testing is also proposed; it can be performed in almost any laboratory. The set-up arrangement is rather simple and requires minimal hardware: a transmitter which send the same packet on a specified communication channel and with a fixed output power, a receiver with the antenna bypassed by an SMA connector and

a low-frequency signal generator which inject disturbance directly in the receiver front-end. With this test, it has been found that 2.4 GHz receivers are particularly susceptible to the injected square waves and it allowed also the derivation of the lowest amplitude causing relevant errors in the communication. For both the BLE and the IEEE 802.15.4 based communications a square wave with 200 mV of amplitude caused a PER> 90%, so the communication can be considered interrupted. Concluding, the so called low-frequency "spurious domain" is an EM polluted environment and the design of RF transceivers should take this into consideration. The antenna selection, the band-pass filter design and also the choice of the LNA-topology should be evaluated at the system design stage considering also the newly introduced low-frequency EMC issue.

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Appendix A

Small signal analysis

A.1 Fluctuation of the bias current of the differential pair

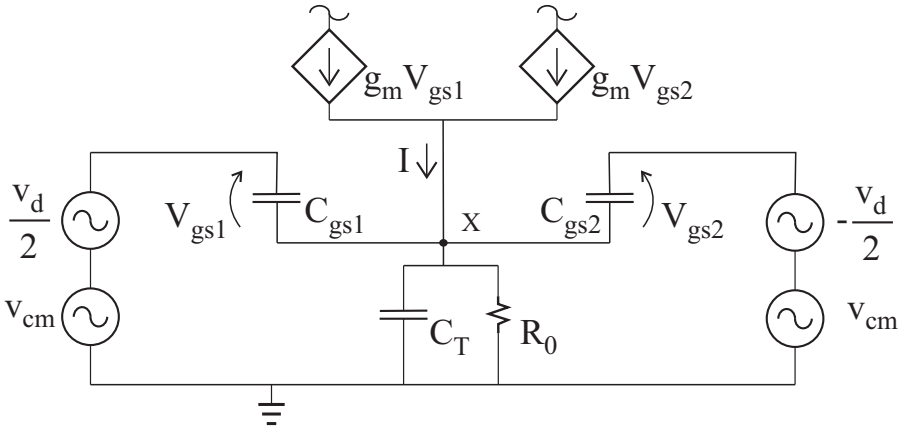

Figure A.1: Differential Pair small-signal equivalent circuit.

Referring to the small-signal equivalent circuit of Fig.A.1, the bias current fluctuation $I(j\omega)$ can be derived by applying Kirchhoff's current law to the common sources' node X:

$$\begin{aligned}&\left(V_{cm}(j\omega)+\frac{V_d(j\omega)}{2}-V_X(j\omega)\right)(j\omega C_{gs1}+g_{m1})+\\&+\left(V_{cm}(j\omega)-\frac{V_d(j\omega)}{2}-V_X(j\omega)\right)(j\omega C_{gs2}+g_{m2})=\\&=V_X(j\omega)\left(j\omega C_T+\frac{1}{R_0}\right)\end{aligned}\tag{A.1}$$

Assuming $g_{m1} = g_{m2} = g_m$ and $C_{gs1} = C_{gs2} = C_{gs}$, the equation simplifies to:

$$(V_{cm}(j\omega) - V_X(j\omega))\,(j\omega 2C_{gs} + 2g_m) = V_X(j\omega)\left(j\omega C_T + \frac{1}{R_0}\right) \tag{A.2}$$

Rearranging the terms in the two sides it reads:

$$V_{cm}(j\omega)R_0\,(j\omega 2C_{gs} + 2g_m) = V_X(j\omega)\,(j\omega R_0[C_T + 2C_{gs}] + 2g_m R_0 + 1) \tag{A.3}$$

$$V_X(j\omega) = \frac{R_0\,(j\omega 2C_{gs} + 2g_m)}{j\omega R_0[C_T + 2C_{gs}] + 2g_m R_0 + 1} V_{cm}(j\omega) \tag{A.4}$$

The expression of the bias current fluctuation become:

$$\begin{aligned} I(j\omega) &= g_m 1\left(V_{cm}(j\omega) + \frac{V_d(j\omega)}{2} - V_X(j\omega)\right) + g_m 2\left(V_{cm}(j\omega) - \frac{V_d(j\omega)}{2} - V_X(j\omega)\right) = \\ &= 2g_m\,(V_{cm}(j\omega) - V_X(j\omega)) = \\ &= 2g_m V_{cm}(j\omega)\left(1 - \frac{R_0\,(j\omega 2C_{gs} + 2g_m)}{j\omega R_0[C_T + 2C_{gs}] + 2g_m R_0 + 1}\right) = \\ &= \frac{2g_m\,(j\omega R_0 C_T + 1)}{j\omega R_0[C_T + 2C_{gs}] + 2g_m R_0 + 1} \end{aligned} \tag{A.5}$$

A.2 Gate to source voltage of the differential pair transistors

The small-signal equivalent circuit of the differential pair of Fig.3.2 is shown in Fig.A.2. The transconductances and the gate to source parasitic capacitances are assumed to be equal ($g_{\mathrm{m\_p}} = g_{\mathrm{m\_m}} = g_m$ and $C_{\mathrm{gs\_p}} = C_{\mathrm{gs\_m}} = C_{\mathrm{gs}}$). The gate

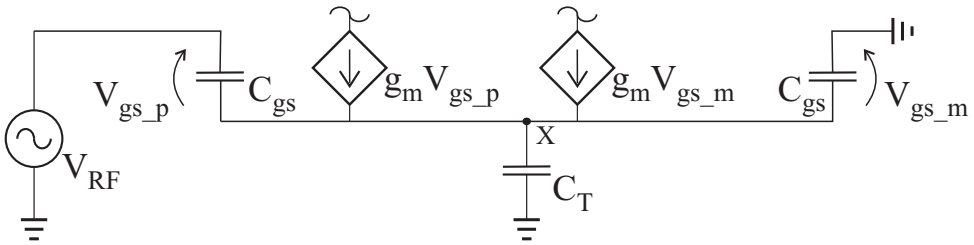

Figure A.2: Differential Pair small-signal equivalent circuit.

to source voltages of the differential pair, namely $V_{\mathrm{gs\_p}}(j\omega)$ and $V_{\mathrm{gs\_m}}(j\omega)$ can be derived by applying Kirchhoff's current law to the node X:

$$(g_m + j\omega C_{\mathrm{gs}})\,V_{\mathrm{gs\_p}}(j\omega) + (g_m + j\omega C_{\mathrm{gs}})\,V_{\mathrm{gs\_m}}(j\omega) = j\omega C_{\mathrm{T}} V_X(j\omega) \tag{A.6}$$

The voltage V_X is then determined by substituting $V_{\mathrm{gs\_p}}(j\omega) = V_{\mathrm{RF}}(j\omega) - V_X(j\omega)$ and $V_{\mathrm{gs\_m}}(j\omega) = -V_X(j\omega)$ and rearranging the equation.

$$(g_m + j\omega C_{\mathrm{gs}})\,(V_{\mathrm{RF}}(j\omega) - V_X(j\omega)) - (g_m + j\omega C_{\mathrm{gs}})\,V_X(j\omega) = j\omega C_{\mathrm{T}} V_X(j\omega) \quad \text{(A.7)}$$

$$(g_m + j\omega C_{\mathrm{gs}})\,V_{\mathrm{RF}}(j\omega) = (2g_m + j\omega[2C_{\mathrm{gs}} + C_{\mathrm{T}}])\,V_X(j\omega) \quad \text{(A.8)}$$

$$V_X(j\omega) = \frac{g_m + j\omega C_{\mathrm{gs}}}{2g_m + j\omega[2C_{\mathrm{gs}} + C_{\mathrm{T}}]} V_{\mathrm{RF}}(j\omega) = -V_{\mathrm{gs\_m}}(j\omega) \quad \text{(A.9)}$$

Finally the gate to source voltage of transistor M_p reads as

$$V_{\mathrm{gs\_p}}(j\omega) = V_{\mathrm{RF}}(j\omega) - V_X(j\omega) = \frac{g_m + j\omega[C_{\mathrm{gs}} + C_{\mathrm{T}}]}{2g_m + j\omega[2C_{\mathrm{gs}} + C_{\mathrm{T}}]} V_{\mathrm{RF}}(j\omega) \quad \text{(A.10)}$$

A.3 Input impedance of the Common Gate LNA

The input impedance R_{CG} of the common gate LNA is determined referring to the equivalent circuit depicted in Fig.A.3.

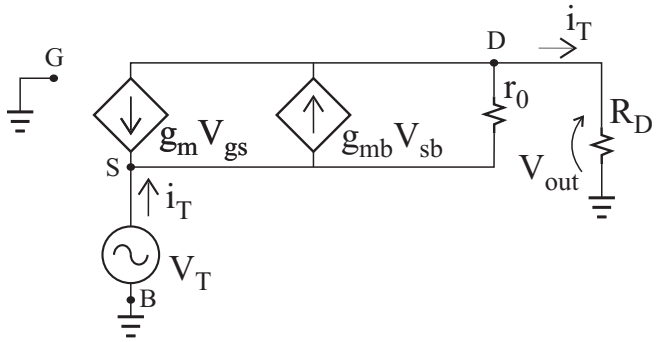

Figure A.3: CG LNA small signal equivalent circuit for the input impedance evaluation.

The test generator V_T is connected between AC ground and the source of the input transistor. The source to body voltage, the gate to source voltage and the drain to source voltage are derived to be:

$$V_T = V_{sb} = -V_{gs} \qquad V_{ds} = i_T R_D - V_T \quad \text{(A.11)}$$

The Kirchhoff's current law is then applied to the source node leading to the following equation:

$$i_T + g_m V_{gs} - g_{mb} V_{sb} + \frac{V_{ds}}{r_0} = 0 \quad \text{(A.12)}$$

The input impedance is evaluated by substituting (A.11) into (A.12) and rearranging terms.

$$i_T - g_m V_T - g_{mb} V_T + \frac{i_T R_D - V_T}{r_0} = 0 \tag{A.13}$$

$$i_T \left(1 + \frac{R_D}{r_0}\right) = V_T \left(g_m + g_{mb} + \frac{1}{r_0}\right) \tag{A.14}$$

$$i_T(r_0 + R_D) = V_T[1 + (g_m + g_{mb})r_0] \tag{A.15}$$

$$R_{CG} = \frac{V_T}{i_T} = \frac{r_0 + R_D}{1 + (g_m + g_{mb})r_0} \tag{A.16}$$

$$\tag{A.17}$$

A.4 Voltage gain of the Common Gate LNA

The voltage gain $A_V = V_{out}/V_{in}$ of the common gate LNA is evaluated analyzing the equivalent circuit depicted in Fig.A.4. The voltage gain is derived calculating

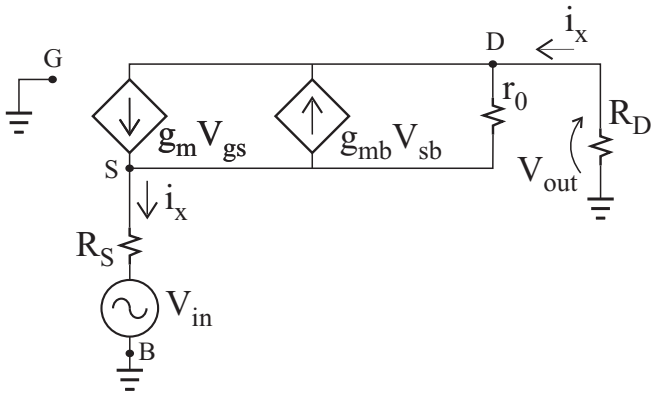

Figure A.4: Common Gate LNA small signal equivalent circuit for the voltage gain evaluation.

the current i_x as a function of V_{in} (KCL at the source node) and substituting its

expression into the output voltage equation, that is $V_{out} = -R_D i_x$.

$$g_m V_{gs} - g_{mb} V_{sb} + \frac{V_{ds}}{r_0} - i_x = 0 \tag{A.18}$$

$$V_{sb} = -V_{gs} = V_{in} + R_S i_x \qquad V_{ds} = -(R_D + R_S) i_x - V_{in} \tag{A.19}$$

$$-(g_m + g_{mb})(V_{in} + R_S i_x) - \frac{(R_D + R_S) i_x + V_{in}}{r_0} - i_x = 0 \tag{A.20}$$

$$-\left(g_m + g_{mb} + \frac{1}{r_0}\right) V_{in} = i_x \left(1 + \frac{R_S}{r_0} + \frac{R_D}{r_0} + (g_m + g_{mb}) R_S\right) \tag{A.21}$$

$$i_x = \frac{(g_m + g_{mb}) r_0 + 1}{(g_m + g_{mb}) r_0 R_S + r_0 + R_D + R_S} V_{in} \tag{A.22}$$

$$V_{out} = -R_D i_x = -\frac{(g_m + g_{mb}) r_0 R_D + R_D}{(g_m + g_{mb}) r_0 R_S + r_0 + R_D + R_S} V_{in} \tag{A.23}$$

A.5 Input impedance of the cascoded CG LNA

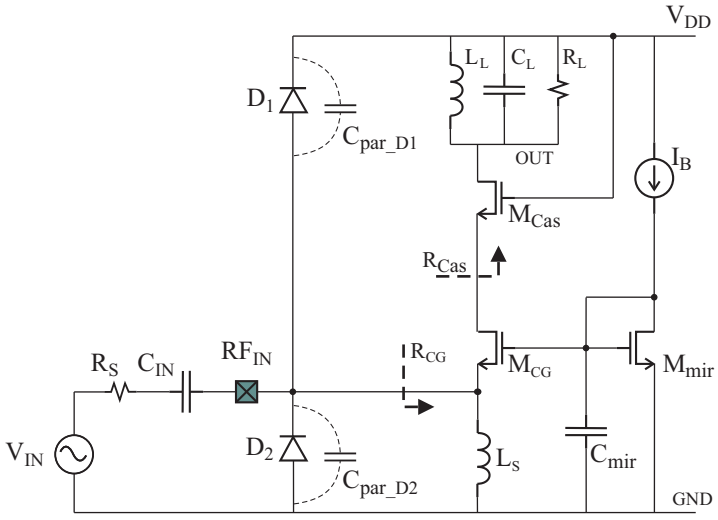

Figure A.5: Designed Common Gate Low Noise Amplifier (CG LNA).

The input resistance of the cascoded CG LNA is derived by evaluating the resistance seen from the drain of M_{CG}. It is the input impedance of the common gate stage (appendix A.3):

$$R_{Cas} = \frac{R_L + r_{0\_Cas}}{1 + (g_m + g_{mb})_{Cas} r_{0\_Cas}} \tag{A.24}$$

This resistance can be seen as the load of another common gate stage, so the resulting input resistance become:

$$R_{CG} = \frac{r_{0\_CG} + R_{Cas}}{1 + (g_m + g_{mb})_{CG}\ r_{0\_CG}} = \tag{A.25}$$

$$= \frac{r_{0\_CG} + \dfrac{R_L + r_{0\_Cas}}{1 + (g_m + g_{mb})_{Cas}\ r_{0\_Cas}}}{1 + (g_m + g_{mb})_{CG}\ r_{0\_CG}} = \tag{A.26}$$

$$= \frac{r_{0\_CG} + (g_m + g_{mb})_{Cas}\ r_{0\_Cas}\ r_{0\_CG} + R_L + r_{0\_Cas}}{[1 + (g_m + g_{mb})_{CG}\ r_{0\_CG}][1 + (g_m + g_{mb})_{Cas}\ r_{0\_Cas}]} \tag{A.27}$$

A.6 Input impedance of the Common Source LNA

The input impedance Z_{IN} of the common source LNA is determined referring to the equivalent circuit depicted in Fig.A.6.

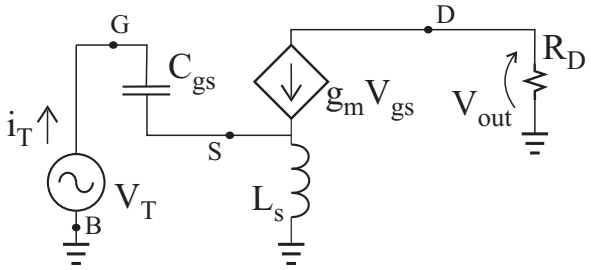

Figure A.6: Common Source LNA small signal equivalent circuit for the input impedance evaluation.

The voltage between the source node and the AC ground is determined by the current flowing into the inductance L_S, that is:

$$V_S = (I_T + g_m V_{gs})\ sL_S \tag{A.28}$$

The gate to source voltage of the input transistor reads:

$$V_{gs} = \frac{1}{sC_{gs}} I_T = V_T - V_S \tag{A.29}$$

The input impedance can be derived by substituting (A.29) into (A.28) and rearranging terms:

$$\frac{1}{sC_{gs}} I_T = V_T - I_T \left(sL_S + \frac{g_m sL_S}{sC_{gs}} \right) I_T \tag{A.30}$$

$$V_T = \left(\frac{1}{sC_{gs}} + sL_S + \frac{g_m sL_S}{sC_{gs}} \right) I_T \tag{A.31}$$

$$Z_{IN} = \frac{V_T}{I_T} = \frac{1}{sC_{gs}} + sL_S + \frac{g_m L_S}{C_{gs}} \tag{A.32}$$

Appendix B

Matlab code

B.1 Input impedance measurement

```
time_5 = timer('TimerFcn','tempus_fugit=0;','StartDelay', 15);

Fstart=10; Fstop=1000; Pow=-10; points=1601;

%Instrument connection
[NetwAna]=NetwAna_ON;

%set the calibration and measurement parameters
fprintf(NetwAna, 'CALK35MD;');                    %select calibration
fprintf(NetwAna, 'RECAREG06;');                   %recall calibration
fprintf(NetwAna, ['POIN ',num2str(points),';']);     %number of points
fprintf(NetwAna, ['STAR ',num2str(Fstart),'MHz;']);  %starting frequency
fprintf(NetwAna, ['STOP ',num2str(Fstop),'MHz;']);   %stop frequency
fprintf(NetwAna, ['POWE ',num2str(Pow),'DB;']);      %RF power in dBm

%select channel and measure
fprintf(NetwAna, 'CHAN1;');
fprintf(NetwAna, 'AUXCOFF;');
fprintf(NetwAna, 'S11;');
fprintf(NetwAna, 'LOGM;');
fprintf(NetwAna, 'CONT');

%select averaged measures
fprintf(NetwAna, 'AVERFACT 16;');
```

```
fprintf(NetwAna, 'AVEROON;');
fprintf(NetwAna, 'AVERREST;');

%wait for averages
start(time_5);
wait(time_5)

%data acquisition
fwrite(NetwAna, 'FORM4; OPC?;');
opc_comp=fscanf(NetwAna);
fwrite(NetwAna, 'OUTPDATA;');
data1=scanstr(NetwAna);

%data re-ordering
mag=zeros(1,points); pha=zeros(1,points); dB=zeros(1,points);
for ind=1:1:points
    mag(1,ind)=data1{(2*ind)-1};
    pha(1,ind)=data1{2*ind};
end

%save data
save([destination,'data.mat'],'freq','mag','pha');

% Disconnect instrument
fclose(NetwAna);

% Clean up all objects.
delete(NetwAna);
clear NetwAna


function [NetwAna]=NetwAna_ON
NetwAna     = instrfind('Type', 'gpib', 'BoardIndex', 0,
                        'PrimaryAddress', 16, 'Tag', '');
if      isempty(NetwAna)     NetwAna=gpib('NI', 0,16);
else    fclose(NetwAna);     NetwAna = NetwAna(1);         end

set(NetwAna,'InputBufferSize', 80050);
set(NetwAna,'OutputBufferSize', 80050);

fopen(NetwAna);
```

```
clrdevice(NetwAna)
fprintf(NetwAna,'*RST;');
return
```

B.2 Interference injection and offset evaluation

```
P_want=[-15,-10,0,5,10];
freq=[(10:2:100),(104:4:400),(450:50:1000)];

V_noDist=zeros(1,length(freq));
V_Dist=zeros(1,length(freq));
V_off=zeros(1,length(freq));

time_2 = timer('TimerFcn','tempus_fugit=0;','StartDelay', 1);

% Read serial port objects:
WaveGen    = instrfind('Type', 'gpib', 'BoardIndex',
                       0, 'PrimaryAddress', 10, 'Tag', '');
Multim     = instrfind('Type', 'gpib', 'BoardIndex',
                       0, 'PrimaryAddress', 24, 'Tag', '');
RF_source  = instrfind('Type', 'gpib', 'BoardIndex',
                       0, 'PrimaryAddress', 19, 'Tag', '');
Pow_meter  = instrfind('Type', 'gpib', 'BoardIndex',
                       0, 'PrimaryAddress', 20, 'Tag', '');

% Create the GPIB objects
if      isempty(WaveGen)    WaveGen=gpib('NI', 0,10);
else    fclose(WaveGen);    WaveGen = WaveGen(1);       end
if      isempty(Multim)     Multim=gpib('NI', 0,24);
else    fclose(Multim);     Multim = Multim(1);         end
if      isempty(RF_source)  RF_source=gpib('NI', 0, 19);
else    fclose(RF_source);  RF_source = RF_source(1);   end
if      isempty(Pow_meter)  Pow_meter=gpib('NI', 0, 20);
else    fclose(Pow_meter);  Pow_meter = Pow_meter(1);   end

% Instruments connection
fopen(WaveGen);     fopen(Multim);
fopen(RF_source);   fopen(Pow_meter);
```

```
% Instruments reset
fprintf(WaveGen,'*RST;');   fprintf(Multim,'*RST;');
fprintf(RF_source,'*RST;'); fprintf(Pow_meter,'*RST;');

% DC bias
fprintf(WaveGen , 'APPL:DC DEF, DEF, 0');

%interference injection and offset calculation
rf_off(RF_source); start(time_2); wait(time_2);
for p_ind=1:1:length(P_want)
    for ind=1:1:length(freq)
        out=query(Multim,'MEAS:VOLT:DC? 25, 0.0001');
        V_noDist(ind)=str2num(out); start(time_2); wait(time_2);
        rf_set(RF_source,freq(ind),DPI_power(ind)); rf_on(RF_source)
        out=query(Multim,'MEAS:VOLT:DC? 25, 0.0001');
        V_Dist(ind)=str2num(out);
        V_off(ind)=V_Dist(ind)-V_noDist(ind);
        rf_off(RF_source); start(time_2); wait(time_2);
    end
    %plot offset and save data
    offs=figure(); semilogx(freq,V_off,'k-*'); grid on
    xlabel('MHz'); ylabel('V');
    title(['Offset voltage vs. frequency,
            constant power= ',num2str(P_want(p_ind)),'dBm'])
    print(offs,'-dpng',[destination,OpAmp,'_off',num2str(P_want(p_ind)),'dBm'])
    save([destination,OpAmp,num2str(P_want(p_ind)),'dBm.mat'],'freq','V_off');
end

% Disconnect all objects.
fclose(WaveGen);
fclose(Multim);
fclose(RF_source);

% Clean up all objects.
delete(WaveGen);
delete(Multim);
delete(RF_source);

function rf_set(RF_source,freq,DPI_power)
fprintf(RF_source,':FREQ %dMHZ;',freq);
```

```
fprintf(RF_source,':POW %dDBM;',DPI_power);
time2 = timer('TimerFcn','tempus_fugit=0;', 'StartDelay', 0.5);
start(time2); wait(time2);
return

function rf_off(RF_source)
fprintf(RF_source,':OUTP OFF');
time2 = timer('TimerFcn','tempus_fugit=0;', 'StartDelay', 0.5);
start(time2); wait(time2);
return

function rf_on(RF_source)
fprintf(RF_source,':OUTP ON');
time2 = timer('TimerFcn','tempus_fugit=0;', 'StartDelay', 0.5);
start(time2); wait(time2);
return
```